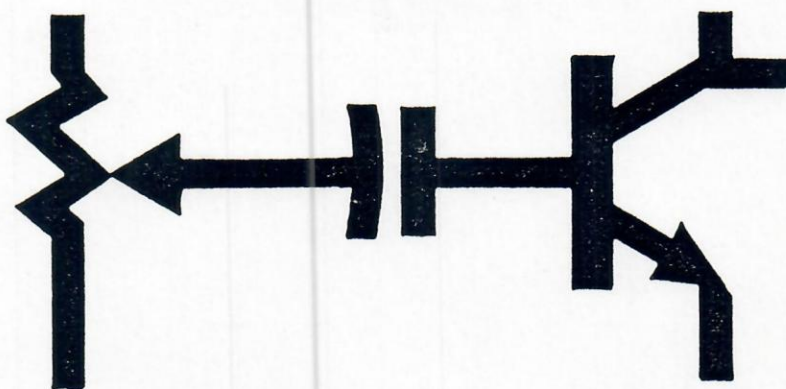


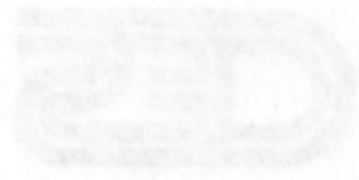


Ed-Lab
ANSWER MANUAL

ELECTRICITY - ELECTRONICS BOOK II



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ELECTRICITY-ELECTRONICS BOOK II

RECTIFIERS and POWER SUPPLIES,
INDUSTRIAL ELECTRONICS CONTROLS,
TRANSISTORS, VACUUM TUBES;
UNITS 4, 5, 6, 7

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CES INDUSTRIES, INC.
Educational Products Division
130 Central Avenue
Farmingdale, New York 11735
Phone (516) 293-1420

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INTRODUCTION

The study of Basic Electricity and Basic Electronics usually includes a dual learning process: 1) Theoretical Study of Concepts and 2) Hands-On Practical Experimentation. The Theoretical Study can consist of Instructor Lectures in the traditional manner, or Self-Study by using a variety of reference materials including text books or audio visual resources in an Individual Instruction or Self-Paced procedure.

The Ed-Lab 650 Training System provides the means for the Circuit Experimentation. The add-on Ed-Lab 101 Prototype Breadboard provides a means for student experiences with a variety of components and circuit board assembly. The Ed-Lab 650 manuals contain the experiment procedures plus the technical explanations needed.

The Ed-Lab 650 Book II, consisting of Units 4, 5, 6 and 7 cover the topics of Rectifiers & Power Supplies, Industrial Electronics, Transistor Circuits and Vacuum Tubes.

All the circuits are practical applications which can be found in many electronics devices ranging from consumer electronics used in Hi Fi, Television, Communications, Telephone and appliance control systems to Industrial Systems, computers and military electronics systems. The student builds and tests the circuits and records the results of each test.

In Unit 4 the student is first introduced to the basic Half Wave Rectifier. From this starting point he builds and test the Full Wave Rectifier, Bridge Rectifier, Power Supply Filters, Regulation, Voltage Control, Zener Regulation, Series Pass Elements, Current Regulation, Feedback Regulation and Operational Amplifier Regulators in a succession of experiments. This progression of

practical circuits is intended to give the student experience in the fabrication, test and troubleshooting of typical Power Supply circuits. Upon completion of the unit the student should be familiar with the bulk of Power Supplies that he will encounter on the job. The same philosophy applies to the units on Industrial Circuits, Transistor Circuits and Vacuum Tubes. The overall effort is to give the student an understanding in electronics circuits to assure his ability to function when he enters into industry.

REFERENCE TEXTS INCLUDE:

Buban & Schmitt; Understanding Electricity & Electronics, McGraw-Hill, 1975

Tepper; Basic Radio, 1 to 7, Hayden, 1973

Mileaf; Electricity 1 to 7, Hayden, 1967

Rutkowski; Solid-State Electronics, Howard W. Sams, 1975

Grob; Basic Electronics, McGraw-Hill 1977 4th Edition

Veatch; Pulse and Switching Circuit Action, McGraw-Hill, 1971

Malvino; Electronic Principles, McGraw-Hill, 1973

Shrader; Electronic Communication, McGraw-Hill, 1975

Gerrish; Electricity and Electronics, Goodheart-Wilcox, 1968

Buban & Schmitt; Technical Electricity & Electronics, McGraw-Hill, 1975

BOOK 11 ELECTRONICS ERRATA SHEET
(FOR EDITION DATED 1978)

UNIT 4

EXP. No. 7

Page 1: Figure 7-1, change the meter scale used from "+10V" to "+50V".

EXP. No. 8

Page 1: Add "+50V" on + input to meter.

EXP. No. 18

Page 1: Figure 18-1, change "+V3" to "+V2"

EXP. No. 19

Page 1: Step 3, in column marked R_L change "20K" to "22K"

UNIT 5

EXP. No. 3

Page 1: Figure 3-1, add connection to GROUND from top of SWITCH C.

EXP. No. 8

Page 1: Step 3, change "Lower +V1" to "Low Input Voltage (10K POT)"

Page 3: Step 10, change " $R_{BB} = 3.3(V_{BB})$ " to " $R_{BB} = 3.3K(V_{B2})$ "
$$\frac{(+V_{B2} - V_{BB})}{\quad} \quad \quad \frac{(V1 - V_{B2})}{\quad}$$

EXP. No. 10

Page 1: Step 2, change "Vary the 100K POT" to Vary the 10K POT."

EXP. No. 12

Page 1: Step 1, remove the second sentence "Use the Vertical... Oscilloscope."

Third sentence change "The Vertical Sweep measures..." to
"The Meter measures..."

EXP. No. 16

Page 1: Step 4, change " $\frac{V_H}{3K}$ " to " $\frac{V_H}{2K}$ " and change " $\frac{V_H}{3}$ " to " $\frac{V_H}{2}$ "

EXP. No. 18

Page 1: Schmeatic, add "100K Resistor from Base of Q7 to Ground"

EXP. No. 19

Page 1: Step 3, change "Please" to "Place"

EXP. No. 26

Page 2: Step 6, line 7, change "SWITCH B UP" to "SWITCH B DOWN"

Page 3: Add the following note to the end of the experiment: Note: The calculations of inductance performed in this experiment ignore the series resistance of the transformer winding and any magnetic or "core" losses and thus have an inaccuracy associated with them but demonstrate the magnitude of the change involved in a saturable reactor device.

UNIT 5
EXP. No. 28

Page 1: Schematic; Change voltage across 100 ohm resistor near +V1 from " $V_{R \text{ D.C.}}$ " to " $V_{R \text{ IN}}$ ".

Step 2; Third column from left, change heading from " $V_{R \text{ D.C.}}$ " to " $V_{R \text{ IN}}$ "

Page 2: Step 3: First line; change " $V_{R \text{ D.C.}}$ " to " $V_{R \text{ IN}}$ "

UNIT 6
EXP. No. 1

Page 3: line 4 change " $I_B = \frac{V_{BR}}{10R} = \frac{V_{BR} \text{ milliamps}}{10}$ "

$$\text{to: } I_B = \frac{V_{BR}}{100K} = \frac{V_{BR}}{100} \text{ ma}$$

line 5 change " $I_B = \frac{V_{BR}}{10} = \frac{0.75}{10} \text{ milliamps}$ "

$$\text{to: } I_B = \frac{V_{BR}}{100} = \frac{0.75}{100} \text{ milliamps}$$

line 6 change " $I_B = \frac{0.75}{10} = 0.075 \text{ ma}$ " to " $I_B = \frac{0.75}{100} = 0.0075 \text{ ma}$ "

EXP. No. 14

Page 1: Figure 14-1 remove connection on bottom right side of schematic shown from +V1 to GROUND.

EXP. No. 15

Page 2: Step 5, line 3, change "Experiment 5, page 5" to "Experiment 5 page 2".

EXP. No. 21

Page 4: Step 5, Add the following Note:

Note: In order to measure the variation in V_{out} the potentiometric voltmeter was used, as described in UNIT I Experiment #14.

EXP. No. 23

Page 1: Figure 23-1 Add diode D5 to the schematic in place of the wire from the base of Q4 to the base of Q3. The Anode is connected to the base of Q4, the Cathode is connected to the base of Q3.

UNIT 6
EXP. No. 25

- Page 1: Description line 1: change "a bar on N type" to "a bar of N type"
line 8: change "The negative gate voltage attracts" to
"The negative gate voltage repels".
line 9: change "toward the junction" to "toward the center".
- Page 2: line 1: change "The construction of an FET is shown in Figure"
to "the construction of a FET is shown in Figure 25-2".
line 2: change "a bar on N-type" to "a bar of N-type"
3rd line from bottom: delete "terminal of the"
- Page 4: 1st line from bottom; change "(See Figure 1-4)" to "(See Figure 25-4)".
last line change "Figure 1-6" to "Figure 25-6".
- Page 7: Step 3: Extend Vertical Scale of Graph #1 to include
10 volts output
- Page 8: Step 3: Extend Vertical Scale of Graph #2 to include
10 volts output

EXP. No. 26

- Page 1: line 1: change "and to measure" to "and measure"

EXP. No. 27

- Page 2: next to "GAIN: box change:
 $R_{s_{gm}} = 10 \cdot 10^3 \cdot 1000 \cdot 10^{-6} = 10^7 \cdot 10^{-6} = 10"$ to
 $R_{s_{gm}} = 10 \times 10^3 \cdot 1000 \times 10^{-6} = 10^7 \times 10^{-6} = 10"$.

EXP. No. 28

- Page 1: line 1: change "Source" to "GATE"

EXP. No. 29

- Page 3: step 5: change "500 ohms" to "1000 ohms"

EXP. No. 30

- Page 2: Table: change "2.3K" to "2.2K"

UNIT 7
EXP. No. 1

- Page 1: Step 2, line 1, change "1K POT" to "10K POT"
- Page 2: Step 3, remove suggested data points from column marked $V_{input}^{(V_G)}$
of the table. Add note: "Select $V_{input}^{(V_G)}$ for accurate
data in the region where $V_{output}^{(V_P)}$ varies with V_G ."

UNIT 7

EXP. No. 2

Page 5: Step 9, line 6, change " $R_L = 4.7K$ " to " $R_L = 22K$ "

Page 6: Step 10, line 5 change " $R_L = 10K$ " to " $R_L = 22K$ "

Step 11, line 2 change "10K" to "100K"

EXP. No. 3

Page 1: Figure 3-1 remove transistor. Indicate wire connections from center of SWITCH B to top of SWITCH A.

Page 2: Step 3, line 3, change " $\frac{8}{10K} = 0.8 \text{ ma}$ " to " $\frac{8}{22K} = 0.35 \text{ ma}$ "

EXP. No. 5

Page 2: Step 2, change "10K POT" to "100K POT"

Step 4, change "10K POT" to "100K POT"

EXP. No. 6

Page 1: Figure 5-1, add notation point "A" to left hand edge of 1 MEG POT (connected to center arm of 10K POT). Add notation point "B" center wiper arm of 1 MEG POT.

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8. Half-Wave Voltage Doubler
9. Voltage Tripler
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* Requires External Transformer Package

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11. Dynamic Amplifier and Phase Splitter
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13. Common Base Amplifier
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15. Cascaded Amplifier
16. PNP Transistor
17. NPN - PNP Cascaded Amplifier
18. Constant Current Source
19. Difference Circuit
20. Difference Amplifier
21. Constant Current Difference Amplifier
22. Darlington Amplifier
23. Audio Driver
24. Feedback Amplifier

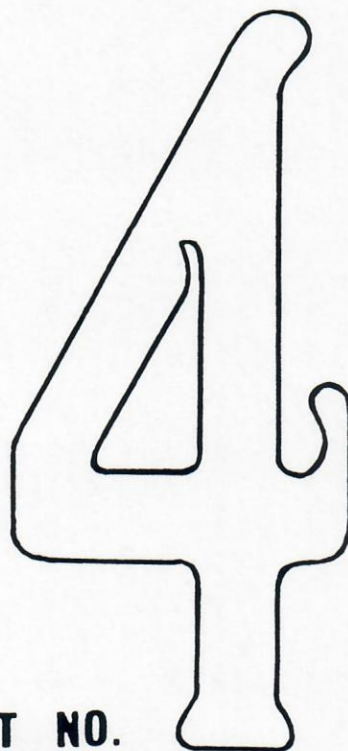
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2. Triode Characteristics
3. Plate Characteristic Curve
4. A.C. Triode Grid Bias Amplifier
5. Cathode Bias
6. Cathode Follower Amplifier
7. Diode Rectifier



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RECTIFIERS & POWER SUPPLIES

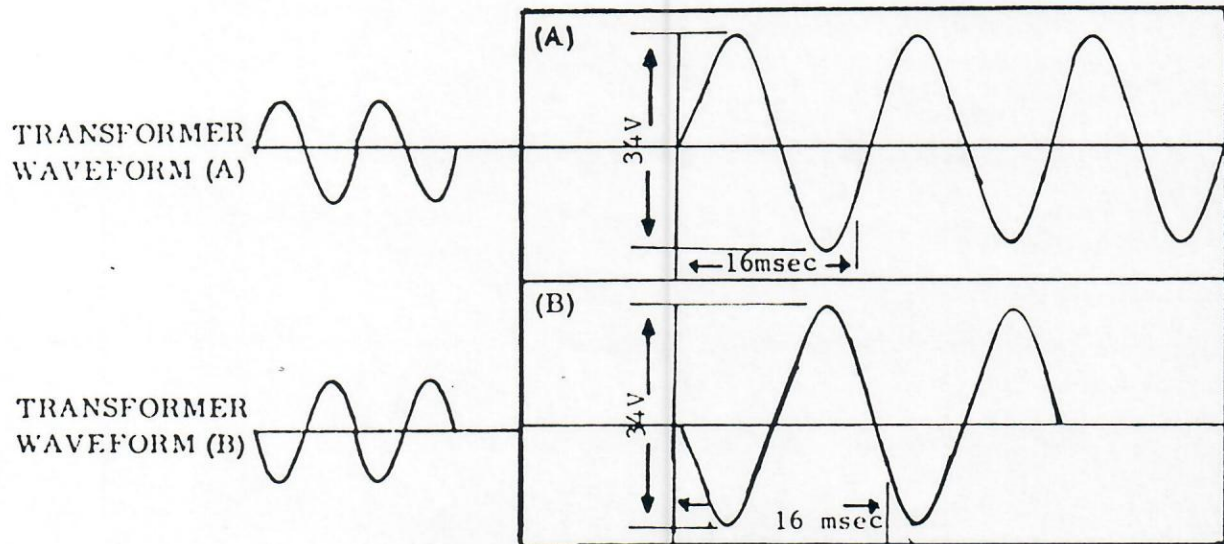


UNIT NO.
CES INDUSTRIES, INC.

TRANSFORMER & HALF WAVE RECTIFIER

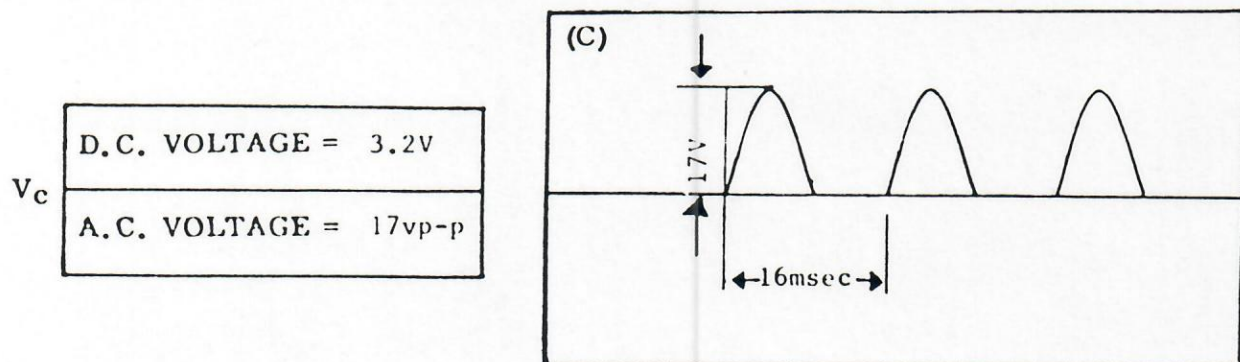
A Half Wave Rectifier Circuit is built and tested. Both positive and negative rectifiers are studied. All voltage waveforms are recorded and the A.C. and D.C. voltage levels are measured.

2.



Note: Without a dual trace oscilloscope or external trigger the waveforms A & B will look alike, actually they are 180° out of phase.

3. Output Waveform

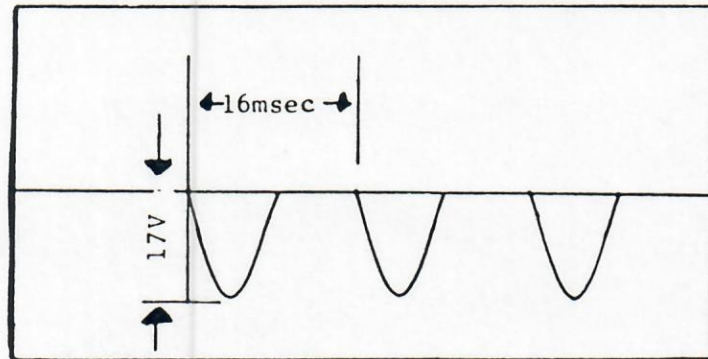


Note: This voltage is recorded in Volts peak to peak. If the meter is used the result will be recorded in Volts RMS by the student.

TRANSFORMER & HALF WAVE RECTIFIER

4. Output Waveforms with the Diode D1 reversed.

V_c	D.C. VOLTAGE = $-3.2v$
	A.C. VOLTAGE = $17vp-p$

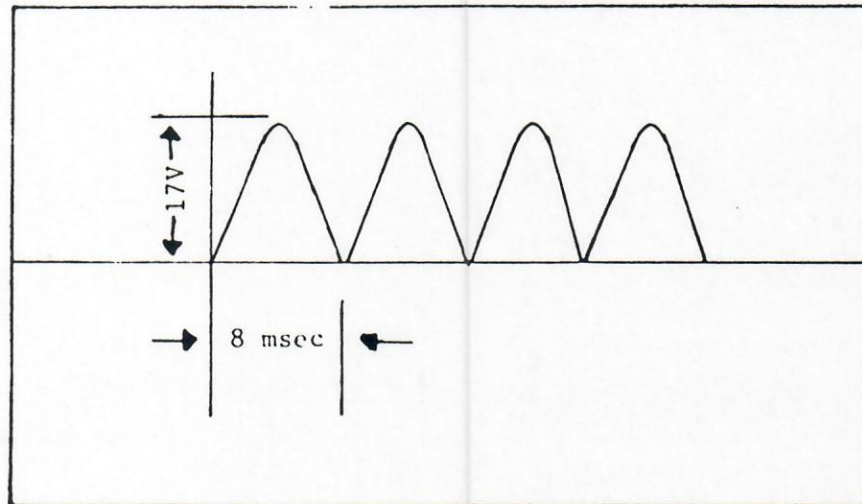


Note: When the diode is reversed the output voltage is negative.

FULL WAVE RECTIFIER

A Full Wave Rectifier is built and tested. The Full Wave and Half Wave Output Voltages are compared.

2.



3. Output Voltages

$V_{A.C.} = 13.0 \text{ VRMS}$	USE ← R. M. S. SCALE
$V_{D.C.} = 6.4 \text{ VDC}$	

4. Comparison of Full Wave and Half Wave Rectifier

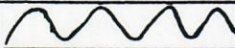
$V_{D.C.} (\text{HALF-WAVE}) = 3.2 \text{ V}$

The Voltage output of the Full Wave Rectifier is twice the voltage output of the Half Wave Rectifier.

FILTER CAPACITOR

Filter capacitors are connected at the output of a full wave rectifier circuit and the filtering effect of different capacitors on the D.C. output is observed. The measurement of A.C. ripple voltages is studied and the calculation of percent ripple is performed.

2.

CAPACITOR	V _{DC}	V _{AC} Ripple	WAVEFORM	
1mfd	8 volts	3 volts p-p		3v p-p
5mfd	9 volts	1 volt p-p		1v p-p
10mfd	9.1 volts	0.5 volts p-p		0.5v p-p
100mfd	9.2 volts	0.1 volts p-p		0.1v p-p

3. For 100 mfd capacitor: Calculation of % ripple.

$$\% \text{ Ripple} = \frac{V_{\text{A.C. ripple}}}{V_{\text{D.C.}}} \times 100 = \frac{0.1}{9.2} \times 100\% = 1.08\%$$

4. Summary of Full Wave Rectifier Voltages with and without filter capacitors.

from Experiment #2 V_{D.C.} (no capacitor) = V(AVE) = 5.4 volts
from Experiment #3 V_{D.C.} (100 mfd capacitor) = V(Peak) = 9.2 volts

5. Calculation of ratio of peak to peak to average voltage.

$$\text{The ratio of } V(\text{peak}) \text{ to } V(\text{average}) = \frac{V_p}{V_{av}} = \frac{9.2}{5.4} = 1.7$$

6. Calculation of the experimental error in Peak/Ave ratio.

$\frac{V_{\text{peak}}}{V_{\text{ave}}}$ compares to 1.57 as:

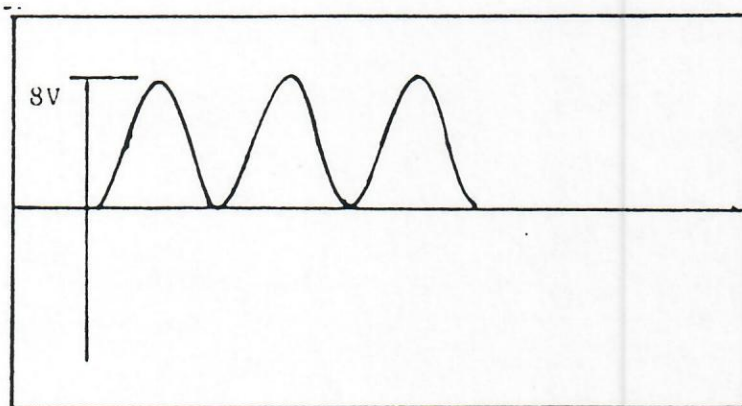
$$\frac{\frac{V_p}{V_{ave}} - 1.57}{1.57} \times 100 = \frac{1.7 - 1.57}{1.57} = 8.2\%$$

The % error between the actual and the theoretical ratio of

$$\frac{V_{\text{peak}}}{V_{\text{ave}}} \text{ is } 8.2\%$$

The waveforms and voltage for a Bridge Rectifier circuit are measured and recorded. Note that in this experiment half the transformer secondary is used. Therefore, the input voltage to the bridge is half that into the Full Wave Rectifier. One important result of this experiment is that the Bridge Rectifier can produce twice the output voltage of the Full Wave Rectifier for a given transformer input voltage.

2. Waveform

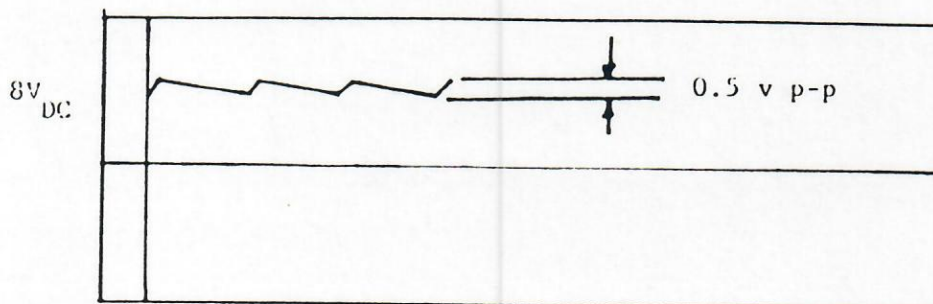


Note: The output voltage is close to the full wave rectifier output voltage with half the input voltage used with the full wave rectifier.

(b)

NO CAP FILTER	V_{DC} (no CAP) =	5 volts
SWITCH A UP	V_{AC} (no CAP)(Scope: peak-to-peak) =	8 v p-p
(optional)	V_{AC} (no CAP)(meter: RMS) =	3.3 VRMS

3. Waveform with Filter Capacitor



BRIDGE RECTIFIER

(b) Voltages

WITH CAP	V_{DC} (Filter cap) = 8 volts
SWITCH A DOWN	V_{AC} (Ripple)(scope: peak-to-peak) = .005 v p-p
(optional)	V_{AC} (Ripple)(meter: RMS) = 0.03 VRMS

4. Comparison of D.C. Voltage output of Full Wave and Bridge Rectifiers.

BRIDGE From (b) above	V_{DC} (Filter Cap) = 8 volts
FULL WAVE From Exp. #3	V_{DC} (with 100 mfd Cap) = 9.2 volts

The voltages are similar but not identical. The differences can be accounted for by the additional diode drops in the Bridge Rectifier System.

REGULATION - FULL WAVE

A load is connected to a full wave rectifier circuit and the effect of loading is measured. The regulation of the full wave rectifier is calculated.

2. NO-LOAD Voltage with SWITCH A UP

$$V_{NL} = 9.1 \text{ volts D.C.}$$

3. Voltage with LOAD (SWITCH A DOWN)

$$V_L = 8.8 \text{ volts D.C.}$$

4. Regulation Calculation

$$\text{REGULATION} = \frac{V_{NL} - V_L}{V_L} \times 100 = \frac{9.1 - 8.8}{8.8} \times 100 = 3.4 \%$$

5. Load Current Calculation using Output Voltage load resistance and Ohms Law.

$$\text{Load Current} = I_L = \frac{V_L}{4.7 \text{ k}} = 1.87 \text{ ma}$$

6. Output Voltage for different loads.

note: in this paragraph, different load resistors are substituted for the 4.7 k load resistor. The 200 load resistor is generated by using the 1 k pot set at 2 divisions as shown in the experiment.

R_{Load}	V_L
no load	9.1 volts D.C.
4.7 K	(repeat) 8.8 volts D.C.
22 K	9.05 volts D.C.
10 K	9 volts D.C.
3.3 K	8.75 volts D.C.
2.2 K	8.6 volts D.C.
1 K	8 volts D.C.
200*	7.1 volts D.C.
100	5.2 volts D.C.

*Use 1K POT set at 2 divisions for 200 Ohms.

REGULATION - FULL WAVE

7. Output Resistance Calculation

(The equivalent resistor in series with an ideal voltage source)

$$\begin{aligned} \text{for } R_L = 100 \Omega & \quad R_0 = \frac{R_L (V_{NL} - V_L)}{V_L} = \frac{100 (9.1 - 5.2)}{5.2} = 75 \Omega \\ \text{for } R_L = 1 \text{ k} \Omega & \quad R_0 = \frac{R_L (V_{NL} - V_L)}{V_L} = \frac{1 \text{ k} (9.1 - 8)}{8} = 130 \Omega \end{aligned}$$

8. Calculation of Regulation for LOAD of 200 ohms

$$\text{REGULATION (200 } \Omega \text{ LOAD)} = \frac{V_{NL} - V_L}{V_L} \times 100 \% = \frac{9.1 - 7.1}{7.1} \times 100 = 28.1 \%$$

V_{NL} = NO LOAD OUTPUT VOLTAGE

V_L = OUTPUT VOLTAGE WITH LOAD

Note: The smaller the value for Regulation the better the quality of the power supply. A power supply with a Regulation of 10% is far inferior to one with a Regulation of 1%

R.C. PI FILTER

An R.C. PI Filter network is compared to the Capacitor Filter. The PI Filter consists of a capacitor filter followed by a low pass R.C. filter so the ripple content of the signal is reduced by the filtering action.

2. Ripple Voltage Measurement

Switch A	Filter	measurement		calculate
		A.C. pk to pk Ripple Voltage	D.C. Voltage	Percentage ripple
DOWN	CAPACITOR	0.3 v	9.1 v	3.3 %
UP	PI (R-C)	0.2 v	9.0 v	2.2 %

3. Calculation of % ripple. % ripple is the percentage of the DC output voltage that the A.C. ripple voltage comprises.

$$\% \text{ RIPPLE} = \frac{V_{\text{A.C. RIPPLE}}}{V_{\text{D.C.}}} \times 100\% = \frac{0.3}{9.1} \times 100 = 3.3\%$$

% RIPPLE CALCULATION FOR PI FILTER

$$\% \text{ RIPPLE} = \frac{V_{\text{A.C. RIPPLE}}}{V_{\text{D.C.}}} \times 100\% = \frac{0.2}{9} \times 100 = 2.2\%$$

NOTE: The PI Filter offers some improvement in the ripple.

4. The advantage of the PI Filter is that it decrease the percent ripple for a rectifier circuit. The reason that the PI Filter is an improvement over the simple Capacitor Filter is because the PI Filter is a LOW PASS FILTER following a Capacitor Filter. The LOW PASS FILTER will filter out an additional amount of A.C. ripple above the simple Capacitor Filter.

$$\% \text{ RIPPLE FOR PI FILTER} = 2.2\%$$

$$\% \text{ RIPPLE FOR CAPACITOR FILTER} = 3.3\%$$

$$\% \text{ IMPROVEMENT} = \frac{\% \text{ Ripple Cap. Filter} - \% \text{ Ripple PI Filter}}{\% \text{ Ripple PI Filter}} \times 100\% = \frac{3.3 - 2.2}{2.2} \times 100 = 50\%$$

NOTE: The PI FILTER configuration is often built with a large inductor in place of the 100 ohm resistor. This is done because the Inductor presents 0 or very small impedance to the D.C. power. Therefore, the regulation of the power supply is not degraded by placing a series inductance at the output of the power supply.

FULL WAVE VOLTAGE DOUBLER

The Full Wave Voltage Doubler is built and the output voltage, A.C. Ripple and % Regulation are measured.

2. Output Voltage & Ripple with no Load (SWITCH A UP)

$$\text{D.C. } V_{NL} = 34\text{v D.C.}$$

$$\text{A.C. } V_{NL} = 0.4\text{v A.C.}$$

3. Output Voltage & Ripple with Load (SWITCH A DOWN)

$$\text{D.C. } V_L = 31\text{v D.C.}$$

$$\text{A.C. } V_L = 0.8\text{v A.C.}$$

4. Voltage Regulation Calculation

$$\% \text{ REGULATION} = \frac{V_{NL} - V_L}{V_L} \times 100 \% = \frac{34 - 31}{31} \times 100 = 9.7 \%$$

5. Ripple Calculation under Load

$$\% \text{ RIPPLE} = \frac{V_L(\text{A.C.})}{V_L(\text{D.C.})} = \frac{0.8}{31} \times 100 = 2.6 \%$$

6. The regulation for the Full Wave Rectifier (Experiment #5) is 3.4%. The regulation for the voltage doubler is 9.7%. The doubler has much poorer regulation than the Full Wave Rectifier.

Note:

The Full Wave Rectifier has a voltage of 9 volts and was taken from the ends of the transformer to the center tap. In this doubler circuit, we take the transformer output from one end to the other and should get double the voltage just from doing this. Therefore, this circuit should really give us four time the voltage for $4 \times 9 = 36$ volts. The output of 34 volts is thus correct, where 2 volts have been lost in various "diode drops."

HALF-WAVE VOLTAGE DOUBLER

A Half Wave Voltage Doubler is built and the output voltage, the A.C. Ripple and Regulation are measured and are compared to the Full Wave Voltage Doubler.

2.

LOAD	D.C. VOLTAGE	A.C. RIPPLE
NO LOAD (Switch A up)	33 v	3 v p-p
LOAD (Switch A down)	29 v	7.5v p-p

3. Calculation of percent Ripple under Load.

$$\text{RIPPLE} = \frac{\text{A.C. RIPPLE}}{V_{D.C.}} \times 100 = \frac{7.5}{29} \times 100 = 25.9 \%$$

Calculation of Regulation

$$\text{REGULATION} = \frac{V_{NL} - V_L}{V_L} \times 100\% = \frac{33 - 29}{29} \times 100 = 13.8\%$$

4. Comparison of Ripple and Regulation for Half Wave Double and Full Wave Doubler.

	Full Wave Doubler	Half Wave Doubler
REGULATION	9.4 %	13.8 %
% Ripple	2.6 %	25.9 %

The Full Wave Voltage has much lower Ripple (factor of 10 improvement in Ripple) and better regulation (46%) improvement over the Half Wave Voltage Doubler.

VOLTAGE TRIPLER

A Voltage Tripler is built and the output voltage is measured.

2. Output Voltage and Ripple Voltage Measurement

$V_{\text{OUTPUT}} = 54 \text{ volts D.C.}$

$V_{\text{RIPPLE}} = 2.5 \text{ v p-p}$

3. Measurement of Voltage Across each capacitor in the Voltage Tripler.

$V_{\text{BA}} = 18 \text{ VOLTS}$	HALF WAVE
$V_{\text{CA}} = 35 \text{ VOLTS D.C. } 35 \text{ V.A.C.}$	DOUBLER
$V_{\text{DA}} = 54 \text{ VOLTS D.C.}$	TRIPLER

Note: There is an A.C. component of voltage across the series capacitors, V_{CA} , as well as a D.C. component.

Note: The Voltage Doubler, Tripler and Quadripler circuits are sensitive to loading. The voltage output will decrease dramatically with increased load. When voltage multiplication is achieved, the regulation suffers.

VOLTAGE QUADRUPLER

A Voltage Quadrupler is built by adding another Diode and Capacitor to the voltage tripler. The main point is that voltage multiplication is accomplished by adding additional stages of doubling circuits.

1. D.C. Voltage Output and A.C. Ripple

D.C. $V_{OUT} = 70$ volts

V_{RIPPLE} (A.C.) = 3 volts p-p

2. Tabulation of the D.C. no Load Voltage Output from the circuits studied preveiously.

Exp. No.	CIRCUIT	VOLTAGE OUTPUT (NO LOAD)	
3	FULL WAVE (with cap)	9.2	} TAKEN ACROSS HALF TRANSFORMER
4	BRIDGE	8.0	
8	HALF-WAVE VOLTAGE DOUBLER	33	} TAKEN ACROSS FULL TRANSFORMER (DOUBLING TO START WITH)
7	FULL-WAVE VOLTAGE DOUBLER	34	
9	VOLTAGE TRIPLER	54	
10	VOLTAGE QUADRUPLER	70	

Note that the current capability of the voltage quadrupler is much lower than the current capability of the transformer. Each time the voltage is multiplied the current output of the circuit is diminished. The load resistor here must be 100K to prevent loading the output voltage down.

ZENER DIODE

The Zener Diode Voltage/Current characteristic is measured and plotted on a graph. This is the first exposure to the Zener Diode and it develops the D.C. characteristic.

2. Zener and Resistor Voltage Measurement

MEASURE		CALCULATE
V_Z	V_R	$I_Z = \frac{V_R}{50} \times 20 \text{ ma.}$
4.1	3.6	72
4.1	3	60
4.05	2.5	50
4.0	2	40
3.9	1.5	30
3.7	1	20
3.4	0.5	10
3.1	0.25	5
0	0	0

Note: V_Z is the voltage across the Zener Diode. V_R is the voltage across the 50 ohm resistor. The resistor voltage is used to calculate the Zener Diode current.

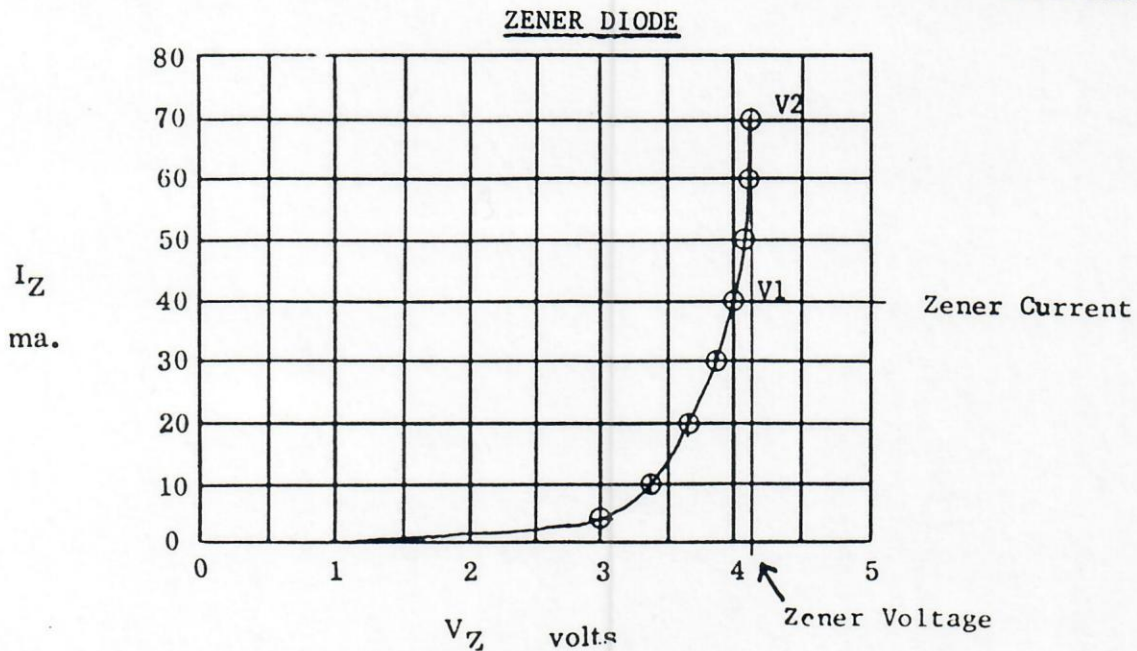
$$I_Z = \text{Zener Current} = \frac{V_R}{50} = V_R \times 20 \text{ ma.}$$

The voltage measurements should be made over the full range of the pot. Only the reverse diode values are measured in this experiment.

3.

$$I_Z = \frac{V_R}{50} = V_R (0.02) \text{ amps} = V_R \times 20 \text{ ma.}$$

4.



5. Zener Voltage Measurement

The Zener Voltage is the constant voltage which the Zener Diode curve approaches for higher currents.

$$V_{ZENER} = 4.1 \text{ volts}$$

6. Minimum Zener Current

The minimum zener current is the smallest current through the Zener diode when the zener is operating at the Zener Voltage. When the zener diode is operating in the Zener Range a large current change will cause only a very small voltage change. This characteristic allows the Zener Diode to be used as a Voltage Regulator.

$$I_{ZENER} = 40 \text{ ma}$$

7. Zener Resistance

The Zener Resistance is the Resistance of the Zener diode when operating in the Zener Range. The Zener Resistance is represented by the slope of the Zener Curve in the Zener range. The more nearly vertical the curve is in the zener range the lower the zener resistance is and the better regulation can be achieved.

$$R_Z = \frac{\Delta V}{\Delta I} = \frac{V_2 - V_1}{I_2 - I_1} = \frac{(4.1 - 4.0) \text{ volts}}{(72 - 40) \text{ ma.}} = 0.003 \text{ kohms}$$

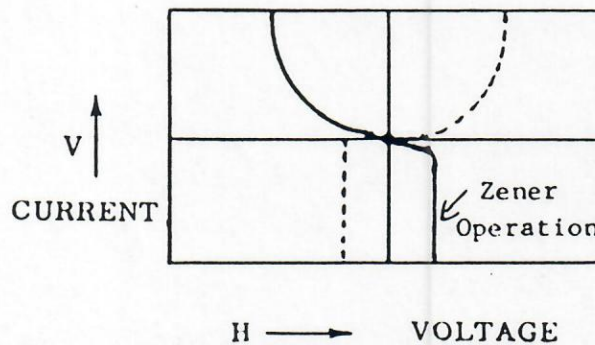
$$R_{ZENER} = 3 \text{ ohms}$$

ZENER CHARACTERISTIC CURVE

In this experiment the A.C. voltage from the transformer is applied to a Resistor and Zener Diode connected in series. The applied A.C. voltage will drive current through the circuit first in one direction, then the other. This will drive the Zener through both the forward and reverse portions of its characteristic curve. The oscilloscope vertical amplifier is connected across the Resistor, so the vertical deflection will be the voltage across the resistor which is proportional to the current flowing in the Zener Diode. The vertical scale therefore represents the Zener Diode Current. The Horizontal Amplifier of the oscilloscope is connected directly across the Zener Diode and will indicate the Zener Voltage on the horizontal scale.

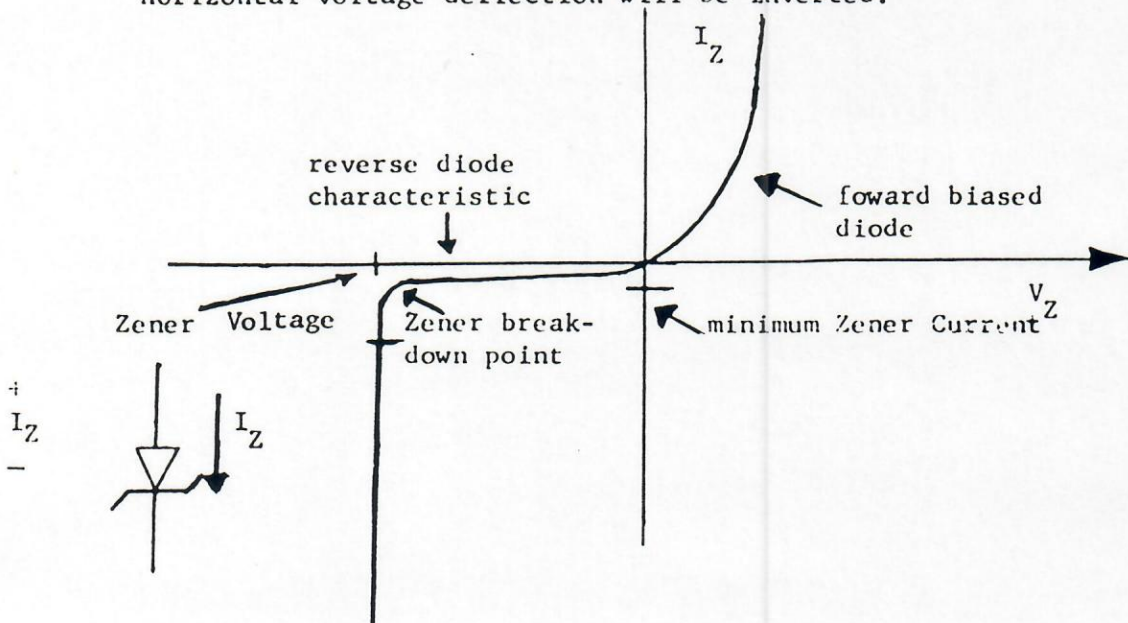
3.

Zener Breakdown Region



Note: Some Oscilloscopes will deflect from Right to Left in the horizontal axis, if the scope sweeps from left to right the solid curve will result. If the scope slews from Right to Left the dotted curve will result.

Note: The horizontal Zener Voltage scale is reversed because the Oscilloscope Common Connection is made to the Junction of the Zener and the resistor. Therefore the horizontal voltage deflection will be inverted.



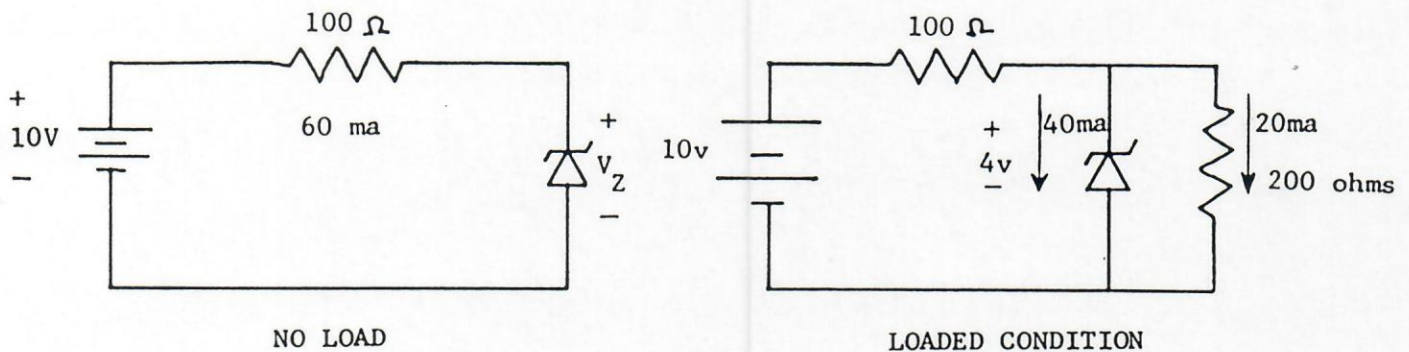
THEORETICAL ZENER CHARACTERISTIC

ZENER REGULATION

The Zener Diode is used as a voltage regulator to regulate a 10 volt D.C. source down to 4 volts D.C. through a 100 ohm series resistor. At no load the current through the 100 ohm resistor will be given by:

$$I = \frac{V_2 - V_{\text{ZENER}}}{100} = \frac{10 - 4}{100} = \frac{6}{100} = 60\text{ma}$$

When a load is introduced onto the output, current will flow in the load. This load current will reduce the amount of current flowing in the Zener diode, but the Zener Diode voltage will not decrease drastically because the Zener Voltage is maintained over a large current range as indicated by the Zener Diode Characteristic, therefore the Zener diode simply has less current flowing through it, at the same voltage.



The regulation will fail when the current demanded by the load at 4 volts reduces the current in the Zener to a value below the Minimum Zener Current.

The slight variation in the Zener voltage under different load conditions is caused by the Zener resistance that acts as a series resistor in the regulator circuit. This Zener resistance applies to the Zener diode when the current through the diode is above the minimum Zener Current.

ZENER REGULATION

2. Data on Zener Regulator

POT POSITION	LOAD	V _{OUT}
1	100	3.6 volts
2	200	3.8 volts
3	300	3.9 volts
4	400	3.9 volts
5	500	3.9 volts
6	600	3.9 volts
7	700	3.9 volts
8	800	3.9 volts
9	900	3.9 volts
10	1000	3.9 volts

NOTE: Somewhere between 200 and 300 ohm load the regulator begins to fail. The load current for these resistances are:

$$I_{LOAD} (200\Omega) = \frac{3.8v}{200} = 19ma$$

$$I_{LOAD} (300\Omega) = \frac{3.9v}{300} = 13ma$$

Since the No Load Current is 60 ma and the Minimum Zener Current is 40 ma as indicated in Experiment #11, we see that the power supply should be able to provide approximately 20 ma before going severely out of regulation.

$$I_{LOAD} (MAXIMUM) = I_{ZENER} (NO LOAD) - I_{MIN. ZENER CURRENT}$$

$$R_{LOAD} (MIN) = \frac{V_{ZENER}}{I_{LOAD} (MAXIMUM)}$$

R_{LOAD} (MIN.) is the smallest load resistor that will not draw more than the maximum Load current at the Zener Voltage.

3. Regulation Calculation

$$Regulation = \frac{(V_{1000} - V_{200})}{V_{200}} \times 100\% = \frac{3.9 - 3.8}{3.8} \times 100 = 2.56\%$$

$$REGULATION = 2.56\%$$

SERIES VARIABLE VOLTAGE

A transistor is used as a Series Pass Element to control the output voltage of a Full Wave Rectifier. The Full Wave Rectifier and Filtered Power Supply output is applied to the collector of the transistor. The base voltage of the transistor is controlled from a voltage divider network. The base voltage biases the transistor ON and the emitter voltage becomes the base voltage less the base-emitter diode drop. Therefore, the Output Voltage is controlled by the Base Voltage. The output current comes mainly through the transistor collector to the emitter and is controlled by the base.

3. Output Voltage plotted versus Control Pot Setting

CONTROL POT	OUTPUT VOLTAGE
0	0 volts
2	1.9 volts
4	3.2 volts
8	6.3 volts
10	7.5 volts

4. Output Voltage plotted versus Load Pot Setting recording.

LOAD SETTING	LOAD R	V _{Output}
2	200	3.0 volts
4	400	3.2 volts
6	600	3.4 volts
8	800	3.45 volts
10	1000	3.5 volts

5. Calculation of REGULATION from 100 ohm load to 200 ohm load.

$$\text{REGULATION} = \frac{(V_{1000} - V_{200})}{V_{200}} \times 100\% = \frac{3.5 - 3.0}{3.0} \times 100\% = 16.7\%$$

Regulation = 16.7%

6. Power Supply Voltage Range. The Power Supply Output Voltage is variable between 0 and 7.5 volts.

At the mid range voltage and 600 ohm load the Ripple is 0.2 volts peak to peak.

8.

Percentage Ripple = $\frac{0.2}{3.4} \times 100\% = 5.8\%$

SERIES REGULATOR

The series variable voltage circuit of experiment #14 is used as a series regulator by using a Zener Diode to set the output voltage. The base voltage is set by the Zener Diode at approximately 4.0 volts. This base voltage sets the emitter voltage at a constant diode drop below 4.0 volts. Since the current drain caused by the transistor base is small compared to the load current the Zener Voltage will remain very constant for varying loads and the output voltage will be well regulated. When the load is large enough to pull the full wave rectifier voltage low enough so the minimum Zener current cannot be provided to the diode the power supply will go out of regulation.

2. Measurement of Output Voltage as a function of load.

LOAD POT	LOAD	V _{OUTPUT}
2	200	3.6 volts
4	400	3.65 volts
6	600	3.65 volts
8	800	3.65 volts
10	1000	3.7 volts

3. The Output Voltage remains constant up to a load of 400 ohms (approximately 10 ma)

4. Regulation Calculation

$$\text{REGULATION} = \frac{V_{1000} - V_{200}}{V_{200}} = \frac{3.7 - 3.6}{3.6} = 2.7\%$$

5. The A.C. Ripple for this circuit is 0.15 volts peak to peak

$$\text{Percentage Ripple} = \frac{0.15}{3.65} \times 100\% = 4.1\%$$

REGULATION MEASUREMENT

The series Regulator is wired and the output voltage variation between no load and full load is measured using a potentiometric voltmeter technique. This technique consists of connecting a voltmeter between the power supply output and a adjustable reference voltage and balancing the meter until it reads mid scale on the 0.5 volts scale. Now any small change in the Power Supply output voltage can be easily seen on the 0.5 volt scale.

5. Measurement of the Balanced Voltmeter with 100 ohm load.

$$V_{1000} = 0.375 \text{ volts}$$

Note: This voltage is set by the student and will vary from report to report.

The Balanced Voltmeter measures 0.3 volts when the load is 300 ohms

6. Calculation of the Output Voltage change from 200 ohm load.

$$\Delta V = \Delta V_{1000} - 0.3 = 0.375 - 0.3 = 0.075 \text{ volts}$$

7. Output Voltage Measurement

$$V_{OUT} = 3.65 \text{ volts}$$

8. Regulation Calculation

$$\text{REGULATION} = R = \frac{\Delta V}{V_{out}} \times 100\% = \frac{0.075}{3.65} \times 100\% = 2\%$$

SHUNT REGULATOR

A full wave rectifier is connected to a shunt transistor which is directly across the Power Supply output. A zener diode is in series with the base circuit to supply a diode voltage reference. With no load the transistor collector is drawing enough current through the 100 ohm resistor to hold the output voltage steady. When a load is connected to the output the Shunt Transistor will draw less current and the load will be supplied with the extra current, maintaining a constant output voltage. The circuit will reach the limit of its regulation when the transistor is drawing no current through the collector and all the power supply current is flowing in the load. An additional load above this level will cause a decrease in the output voltage. Note that in the region of regulation the current in the 100 ohm series resistor remains the same and it is divided between the Shunt Transistor and load the provide V_{out} equal to the diode voltage.

In this experiment the potentiometric method of Regulation measurement is used to measure the small variations in output voltage as the load changes. Since the base current is relatively small, the Zener will not be operating in the breakdown region and the voltage will actually be about 1 volts.

2. Output Voltage Measurement.

$$V_{output} = 1 \text{ volt}$$

NOTE: This voltage may be different on various trainers. The important thing is to measure the Output Voltage and to record as a reference.

3. Tabulation of Load versus Voltage change.

LOAD POT	LOAD	Relative Voltage 0.5 SCALE
2	200	0.3 volts
4	400	0.32 volts
6	600	0.33 volts
8	800	0.35 volts
10	1000	0.35 volts

Note: The Voltages tabulated are not the actual supply output voltage. These voltage readings are the values on the 0.5 volt potentiometric voltmeter scale.

4. Regulation Calculation

$$\text{Regulation} = \frac{(V_{1000} - V_{200})}{V_{output (200)}} \times 100\% = \frac{0.335 - 0.3}{1} \times 100 = \frac{0.035}{1} \times 100\% = 3.5\%$$

$$\text{REGULATION} = 3.5\%$$

FEEDBACK REGULATION

A full wave rectifier circuit is regulated by a series pass transistor Q 4. The current flowing through the series pass element into the load is controlled by the Control Transistor Q 5. The control transistor has its emitter voltage rigidly set by the Zener Diode. Note that the Zener diode gets its current from the output of the regulator, so the Zener voltage is very stable. The 10 K pot is a voltage divider which is used to set the output voltage. When the output voltage is low, the voltage to the base of Q 5 is less than the Zener voltage and Q 5 is biased off. No current will flow in the collector of Q 5 and the series pass transistor, Q 4, will be turned on by the base current flowing in the collector-base 1K resistor. This current flow will cause the output voltage to increase to the correct level.

If the output voltage is too high the voltage on the base of Q 5 will be higher than the Zener voltage and Q 5 will be conducting current in its collector. The current in the collector of Q 5 will be drawn from the base circuit of the series pass element Q 4 and will cause the current flowing to the load through Q 4 to decrease. This decrease in current to the load will cause the output voltage to decrease to the correct level. The series pass element will control the current to the load so that the output voltage will remain at the level which will cause the base voltage to Q 5 to equal the Zener voltage, with Q 5 partly on. Note that a change in the output voltage causes the series pass element to oppose the change and return the circuit to the operating voltage. This is the process of feedback which is used to regulate the supply.

2. Measurement of the output voltage range of adjustment.

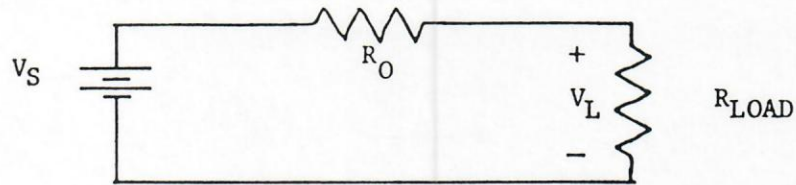
V _{maximum} = 6.0 volts
V _{minimum} = 3.4 volts

3. Measurement of output voltage variations caused by variations of load resistance. V_{out} is set at nominal 4.0 volts. Relative V_{out} refers to the variations of the output voltage from 4.0 volts using a balance meter measurement technique.

LOAD POT	LOAD	Relative V _{out}
Disconnect	NO LOAD	0.3. volts
2	200	0.24 volts
4	400	0.27 volts
6	600	0.28 volts
8	800	0.29 volts
10	1000	0.29 volts

FEEDBACK REGULATION

4. Calculation of Power Supply Output Resistance. Power Supply Output Resistance is the equivalent series resistance in series and Ideal Voltage Source of 4.0 volts.



In order to find the Power Supply Resistance we must measure the output voltage with no load and the output voltage at some known load and then perform the following calculation.

$$V_{NL} = V_S \quad V_L = \frac{V_S R_L}{R + R} \quad V_L = \frac{V_{NL} R_L}{R_L + R_O}$$

$$(R_L + R_O) V_L = V_{NL}$$

$$R_L V_L + R_O V_L + R_L V_{NL}$$

$$R_O V_L = R_L V_{NL} - R_L V_L = R_L (V_{NL} - V_L)$$

$$R_O = \frac{R_L (V_{NL} - V_L)}{V_L}$$

V_{NL} = No Load Supply Voltage
 V_S = Source Voltage
 V_L = Loaded Output Voltage
 R_L = Load Resistance
 R_O = Power Supply Resistance

Using the values in the experiment we know that $R_L = 600$ ohms. The Relative V_{out} is 0.31 volts when the Power Supply is set to 4.0 volts with no load. When the 600 ohms load is on the circuit the relative V_{out} is 0.28 volts which is 0.03 volts less output voltage, meaning that $V_L = 3.97$ volts. The calculation is as follows:

$$R_{OUTPUT} = R_L \frac{(V_{NL} - V_L)}{V_L} = 600 \left[\frac{4.0 - 3.97}{3.97} \right] = 4.5 \text{ ohm}$$

5. Calculation of Power Supply Regulation

$$\text{Regulation} = \frac{(V_{1000} - V_{200})}{V_{200}} \times 100\%$$

(relative V_{out})
(absolute)

$$V_{200} \text{ is } 0.31 - 0.24 = 0.07 \text{ volts less than 4.0 volts} = 3.93 \text{ volts}$$

V_{200} = Output Voltage with 200 ohm load
 V_{1000} = Output Voltage with 1000 ohm load

FEEDBACK REGULATION

$$\text{Regulation} = \frac{(0.29 - 0.24)}{3.93} \times 100 = 1.3\%$$

6. Ripple Voltage Measurement with 1000 ohms load and 5 volt output voltage

$$V_{\text{ripple}} = 0.05 \text{ volts p-p}$$

7. Percentage Ripple Calculation

$$\% \text{ Ripple} = \frac{\text{Ripple Voltage}}{\text{D.C. Voltage}} \times 100 = \frac{0.05}{5} \times 100 = 1\%$$

CURRENT REGULATOR

In this experiment a series pass transistor is used to regulate the current provided to a load. The circuit current is maintained at a constant level by holding the base-emitter circuit voltage constant with a Zener Diode. A constant base-emitter circuit voltage and the fixed emitter resistor will keep the base current steady and therefore, the collector or output current will remain constant.

1. Calculation of Emitter and Collector Current flowing in the 2.2K emitter resistor (base emitter voltage drop and α are neglected.)

$I_C = \frac{V_Z}{2.2K}$	$= \frac{4.0 \text{ (Zener Voltage)}}{2.2}$	ma	$= 1.8 \text{ ma}$
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3. Tabulation of Output Voltage for various load resistors and calculation of output current.

R_L	measure V_{out}	calculate $I_L = \frac{V_{out}}{R_L}$
100	0.14 v	1.4 ma
1K	1.4 v	1.4 ma
2.2K	3.0 v	1.36 ma
4.7K	3.0 v	0.638 ma
10K	3.1 v	0.31 ma
15K	3.0 v	0.2 ma
20K	3.0 v	0.136 ma
33K	3.0 v	0.09 ma
56K	3.0 v	0.05 ma

NOTE: The actual Zener Voltage may not be 4.0 volts. The important thing is that the current for the smaller resistances should remain constant. The Zener used for this experiment was operating at 3.7 volts

4. Calculation of the Maximum Load Resistance which will allow the current regulator to provide its correct regulated current output.

$R_{L \text{ max}} = \frac{V_{\text{max}}}{I_C} = \frac{3 \text{ volts}}{1.8 \text{ ma}} = 1665 \text{ ohms}$

Note: The actual current was 1.4ma. $R_{L \text{ max}} = \frac{3}{1.4 \text{ ma}} = 2.14K \text{ ohms}$

The 3.0 volts V_{max} maximum achievable load voltage results from the maximum rectifier voltage output of 7 volts minus the Zener Diode voltage of 4.0 volts.

5. The calculated maximum resistance is 1665 ohms. Experimentally we see the constant current drop off between load resistances of 2.2K and 1K. Therefore, the experimental results agree with the calculation.

OP-AMP REGULATOR

In this regulator circuit the power supply output voltage is compared to the voltage of a Zener diode using an operational amplifier. The OP-AMP output is then applied to the base of a series pass transistor to keep the output voltage constant at the Zener voltage. The 10K pot is a voltage divider and allows the actual output voltage to be adjusted above the Zener voltage. The Zener is driven from the regulated voltage output so it is a very stable voltage reference. This stable voltage reference and the high gain of the Operational Amplifier will provide very accurate voltage regulation over a wide voltage range. A balanced meter measurement is used to measure variation in the output voltage with change in loads. This is necessary because the output variations will be very small for this regulator.

2. Measurement of Maximum and Minimum output voltage.

$V_{\max} =$	5.5 volts
$V_{\min} =$	1.0 volts

3. Measurement of Output Voltage for various load resistors with 4.0 volts regulator output. Note that the balanced meter is used on the 0.5 volt scale to allow measurement of small variations below 4.0 volts D.C. output.

LOAD POT	LOAD	Relative V_{output}
1	100	0.3 volts
2	200	0.3 volts
4	400	0.3 volts
6	600	0.3 volts
8	800	0.3 volts
10	1000	0.3 volts

NOTE: The Relative Voltage is selected by the student and may differ from this voltage. The important thing is the noted variation in the Relative V_{output} with load changes.

Note: The change in output voltage with load change is so small it cannot be detected with the 0.5 volt meter. Perhaps, by using a more sensitive meter, the voltage variation can be detected. If a very sensitive meter is available, you could try to measure the voltage variation.

OP-AMP REGULATOR

4. Since we could not read any voltage variation on the meter, we must calculate regulation as "better than" the minimum voltage variation we are able to measure. Using the meter on the 0.5 volt scale, each small division represents 0.01 volts. Assuming that we could detect a change of $\frac{1}{2}$ of a small division we can say that the output voltage changed less than 0.005 volts over the range of loads applied. Therefore, we can calculate the voltage regulation as:

$$\text{Regulation is better than } \frac{V_{1000} - V_{200}}{V_{200}} \times 100 = \frac{4 - 3.995}{4} \times 100 \%$$

Regulation = better than 0.12%

5. In the ripple measurement, no ripple voltage will be detected using ordinary instruments, so we must estimate the minimum ripple that we would be able to detect and report the ripple as "less than." With the instruments we used to measure ripple we could measure ripple as low as 0.002 volts so the ripple is less than 0.002 volts.

V ripple = less than 0.002 volts

6. Power Supply Regulator Summary

<u>Power Supply</u>	<u>Experiment</u>	<u>Regulation %</u>
Full Wave Supply (200 ohm load)	5 Paragraph 8	30%
Zener Regulator	13	2.56%
Series Transistor	14	16.7%
Series Transistor with Zener	16	2.7%
Shunt Transistor Regulator with Zener	17	3.5%
Feedback Regulator Transistor	18	1.3%
OP-AMP Regulator	20	Better than 0.12%

POWER SUPPLY EFFICIENCY

A Full Wave Bridge Rectifier is used to drive a series transistor regulator. The series transistor regulator has a voltage control that allows the output voltage to be adjusted from 0 volts to full output voltage. The experiment is to measure the efficiency of this power supply when the voltage is set to about half of full voltage output.

4. Voltage Measurements for half voltage

V_T	=	5.5 volts
V_R	=	3.5 volts
V_L	=	3.6 volts

V_T = Emitter Collector Voltage

V_R = Voltage Across 100ohms load Resistor

V_L = Voltage Across Load Lamp

5. Load Current Calculation

The load current is calculated using the voltage across the 100ohm resistor and ohms law.

$$I_L = \frac{V_R}{100} = 35 \text{ ma}$$

I_L = Load Current

6. Load Power is calculated by multiplying Load Current and Load Voltage.

$$P_L = V_L I_L = (7.2) (50 \times 10^{-3}) = 360 \text{ milliwatts}$$

$$P_L = 0.36 \text{ watt}$$

7. Transistor Power is given by the Collector to Emitter voltage multiplied by the Load Current.

$$P_T = V_T I_L = (7.3) (50 \times 10^{-3}) = 365 \text{ millivolts}$$

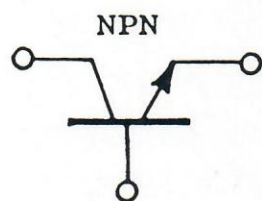
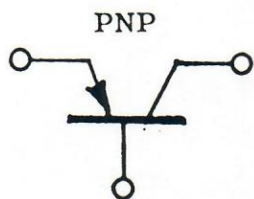
$$P_T = 0.365 \text{ watts}$$

8. Power Supply Efficiency is given by:

$$E = \frac{P_L}{P_L + P_T} = \frac{360}{360 + 365} \times 100\% = 49\%$$

COLLECTOR OUTPUT POWER

In this experiment two power supplies are constructed and tested, one using an NPN series pass transistor and the other using a PNP series pass transistor. The achievable variation in output voltage is measured.



POT POSITION	PNP transistor and 15K resistor	NPN transistor NO BASE resistor
0	11	0
1	11	1.3
2	11	2.8
3	11	4.5
4	11	6
5	10	6.9
6	9.9	7.9
7	9.0	9.0
8	7.6	9.8
9	4.2	11
10	2.0	11

4. The NPN circuit offers better voltage control over a larger range of POT adjustment of the voltage all the way down to "0" volts. This improved control is a function of the fact that the NPN transistor has the output voltage on the emitter so that the emitter voltage tracks the base voltage and the output is as linear as the POT adjustment.

DARLINGTON SERIES REGULATOR

A Full Wave Rectifier with a series pass transistor regulator consisting of a Darlington pair of transistors is built. This Darlington configuration is used because the base current into the base of Q6 is amplified by the Beta of the transistor and injected into the base of the series pass transistor Q7 where it is again amplified by Beta. Therefore, high output currents can be driven from Q7 with very low base current into the base of Q6 for control. This type of regulator is very good for high current power supply regulators.

3. With the lamp on and the 100k POT in position 8, the voltage measurements are:

V_R	3.0 volts
V_L	7.0 volts
V_Y	4.0 volts
V_C	11.5 volts

4. The load current is calculated using the voltage across the 100 ohm resistor and OHM's LAW.

$$I_L = \frac{V_R}{100} = \frac{3.0}{100} = 30 \text{ ma}$$

$I_L = 30 \text{ ma}$

5. The transistor base driving current is calculated by measuring the voltage to the common at both ends of the 470K base resistor. The voltage across the resistor is then the difference between these two voltages. Base driving current is calculated using the voltage across the 470K resistor and OHM's LAW.

$$I_D = \frac{(V_Y - V_C)}{470K} = \frac{11.5 - 4.0}{470K} = \frac{7.5}{470K} = 16 \mu \text{ amps}$$

$I_D = 16 \mu \text{ amps}$

DARLINGTON SERIES REGULATOR

6. Current Gain for the Darlington pair is calculated by dividing the load current by the base driving current.

$$G = \frac{I_L}{I_D} = \frac{30\text{ma}}{16\text{ma}} = \frac{30,000}{16} = 1,875$$

$G = 1,875$

Very High Current Gain



Ed-Lab
ANSWER MANUAL

INDUSTRIAL ELECTRONICS CONTROLS

5

UNIT NO.
CES INDUSTRIES, INC.

TRANSISTOR SWITCH

A switch controlling the current into the Base of an NPN transistor is used to turn ON and OFF a lamp located in the Collector. This experiment shows that a small current in the Base of a transistor controls a large current in the collector of the transistor.

2.

SWITCH A	TRANSISTOR SWITCH	COLLECTOR VOLTAGE	LAMP (ON OR OFF)
UP	CLOSED	0.0	ON
DOWN	OPEN	10.0	OFF

3. Calculation of Base Current and Collector Current

$V_B = 9.1 \text{ VDC}$	$I_B = \frac{V_B}{10,000} = 0.91 \text{ ma}$
$V_C = 3.0 \text{ VDC}$	$I_C = \frac{V_C}{100} = 30 \text{ ma}$

6. Measurement of Base and Collector voltage and current for medium lamp brightness.
(Note: The purpose of adjusting the lamp to medium brightness is to insure that the transistor is operating in the Linear Region. This is required because the current Gain will be calculated in the next step. If the transistor is saturated the current gain will be incorrect)

$V_B = 2.5 \text{ VDC}$	$I_B = 0.25 \text{ ma}$
$V_C = 2.6 \text{ VDC}$	$I_C = 26 \text{ ma}$

7. Calculation of Current Gain.

$\text{CURRENT GAIN} = \frac{I_C}{I_B} = \frac{26}{0.25} \approx 100$

PNPN SWITCH

This experiment demonstrates the operation of a Latching Circuit. It is particularly interesting to note that this circuit operates similarly to an SCR and can be used to explain the operation of the SCR (4 Layer Device). Note that the Semiconductor layers shown in the upper right hand corner of Figure 2-1 are PNPN - the same as the layers in an SCR.

7. Does the circuit operate as a "latching" switch? YES

After the GATE has been energized the circuit will turn ON and remain ON. In order to turn the circuit OFF the GATE voltage must be removed and the Lamp Current must be interrupted. This is also true of the SCR.

SCR SOLID-STATE SWITCH

This experiment constitutes a STATIC or D.C. test of the SCR. The purpose is to allow the student to operate and understand the SCR before using it in an A.C. control circuit. The fact that a large lamp current is controlled by a small gate current is demonstrated. Two methods of turning OFF an SCR circuit are studied, interrupting the Anode Current and Shorting the SCR Anode to Cathode. This demonstrates that the SCR will turn OFF when the current through the SCR drops to Zero momentarily.

2. Set Switch C DOWN, then UP. Does the lamp turn ON and remain ON? YES
3. Set Switch A DOWN, then UP. Does the lamp turn OFF? YES
4. Set Switch C DOWN, then UP to turn the lamp ON. Set Switch B DOWN, then UP. Does the lamp turn OFF? YES
6. Measurement of Turn ON Voltage at the SCR Gate.

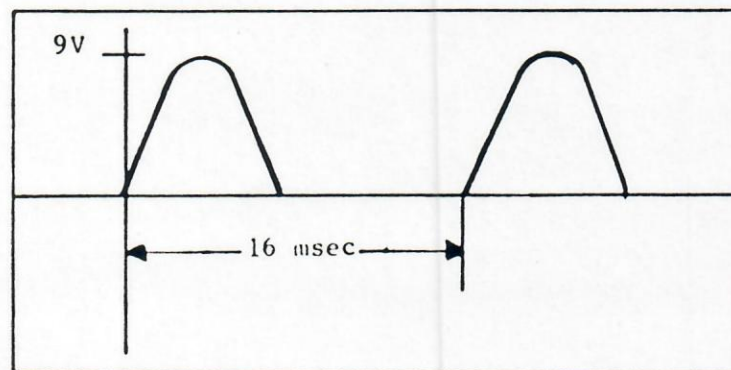
$$V_{in} \text{ (at turn-on)} = 0.3 \text{ VDC}$$

Note: There may be a variation in this turn on voltage in different trainers.

8. Turn On Voltage with A.C. Anode Supply

$$V_{in} \text{ (TURN-ON)} = 0.3 \text{ volts D.C}$$

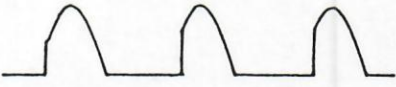
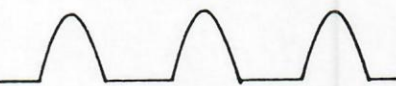
9. Output Waveform.



SCR RECTIFIER CONTROL SWITCH

This is a DYNAMIC or A.C. application of the SCR which introduces the student to the most basic use of the SCR to control A.C. power. In A.C. applications of this type, it is not necessary to manually turn the SCR OFF. When the A.C. Input Voltage passes through Zero the SCR will turn OFF. Note that the load power flows in the SCR Anode circuit while the GATE current is small.

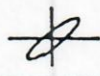
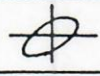
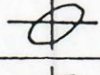
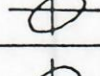
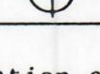
2. Waveforms for various lamp intensities.

LAMP	WAVEFORM	D.C. Volts (Average)
DIM		2.5 VDC
MEDIUM		4.0 VDC
BRIGHT		5 VDC

R - C PHASE SHIFT

This experiment constitutes a review of Phase Shift and presents the R-C Phase Shift circuit in the form that it is used in driving the GATE of an SCR controller circuit.

2. Lissajou Pattern Data

100K POT Position	LISSAJOUS PATTERN	Lissajous		
		A	B	C
0		4.0	0.1	9.4
2		4.0	3.0	5.0
4		4.0	3.6	2.4
6		4.0	3.8	1.6
8		4.0	3.8	1.2
10		4.0	3.9	1.0

6. What are the phase-shift and the attenuation at POT setting 0?

$$\theta = \arcsin \left(\frac{B}{A} \right) = \arcsin \frac{0.1}{4.0} = 1.43^\circ; \text{ Attenuation} = \frac{C}{A} = \frac{9.4}{4} = 2.35$$

7. What are the maximum phase-shift and maximum attenuation at POT setting 10?

$$\theta = \arcsin \left(\frac{B}{A} \right) = \arcsin \frac{3.9}{4.0} = 77^\circ; \text{ Attenuation} = \frac{C}{A} = \frac{1}{4} = 0.25$$

It would be very desirable to use a Dual Trace Oscilloscope.

PHASE SHIFT SCR CONTROL

This is an actual application of the SCR as an A.C. controller. Note that both the attenuation and the R - C Phase Shift contribute to the delay in the SCR turn on point. This combination allows the SCR to control the A.C. wave throughout the full 180° Half Cycle.

2. Waveforms

LAMP	WAVEFORM	D.C. VOLTS
DIM		0.9 VDC
MEDIUM		2.5 VDC
BRIGHT		5.0 VDC

3. D.C. Voltage Range

$V_{\max} = 5.0 \text{ VDC}$ $V_{\min} = 0.85 \text{ VDC}$
--

4. Place another 0.25 mfd cap in parallel with C. What is $V_{\min}$?

$$V_{\min} = 0.2 \text{ VDC}$$

5. Replace the 100K POT with 1M POT. What is $V_{\min}$?

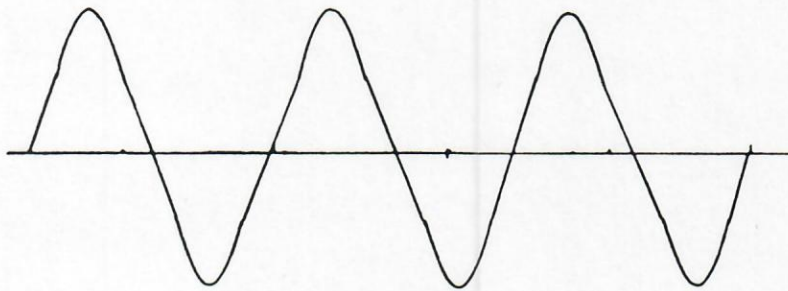
$$V_{\min} = 0.0 \text{ VDC}$$

SCR STATIC CONTROL

In this experiment the SCR is used to control a load. The GATE or control input is very low current (the gate circuit is in series with a 100K resistor). This means that a low power switch (Switches A and B) can control a high power load via an SCR. This circuit is used in industry to control high power motors. A small, low current switch may be used and the switch lifetime is extended because the main current is not switched by the mechanical control switch, but is controlled by the SCR.

2. Set Switch A UP, then DOWN. A positive voltage on the gate will turn the SCR ON.
Does the lamp turn on? YES
3. Does the Lamp turn OFF? YES
5. Is the lamp OFF? YES
6. Set Switch A UP. Is the lamp ON? YES

DUAL. SCR (AC) WAVEFORM



UNIUNCTION TRANSISTOR

A STATIC or D.C. test is performed on the Unijunction Transistor. The Intrinsic Stand-Off Ratio and the Interbase Resistance are measured. The purpose is to familiarize the student with the features and operation of the Unijunction Transistor.

2. Emitter Voltage at the point of conduction.

$$V_C = 4.8 \text{ VDC}$$

3. Supply Voltage measurement

$$V_{B2} = 6.4 \text{ VDC}$$

4. Calculation of η . (Eta).

$$\eta = 0.75$$

5. Measurement of η for a different supply voltage

$$\eta = \frac{V_C}{V_{B2}} = \frac{(2.5)}{(3.2)} = 0.78$$

Note: The value of η does not depend upon the supply voltage. η will be a constant for all Source Voltages and is a Ratio.

6. How does this value of ETA compare with that calculated in step 4 above?

They are the same to within the accuracy of measurement

7. Measurement of V_{B2} with Unijunction Transistor OFF.

$$V_{B2} = 6.4$$

9. Supply Voltage Measurement

$$+V1 = 9.8 \text{ VDC}$$

10. Calculation of Interbase Resistance

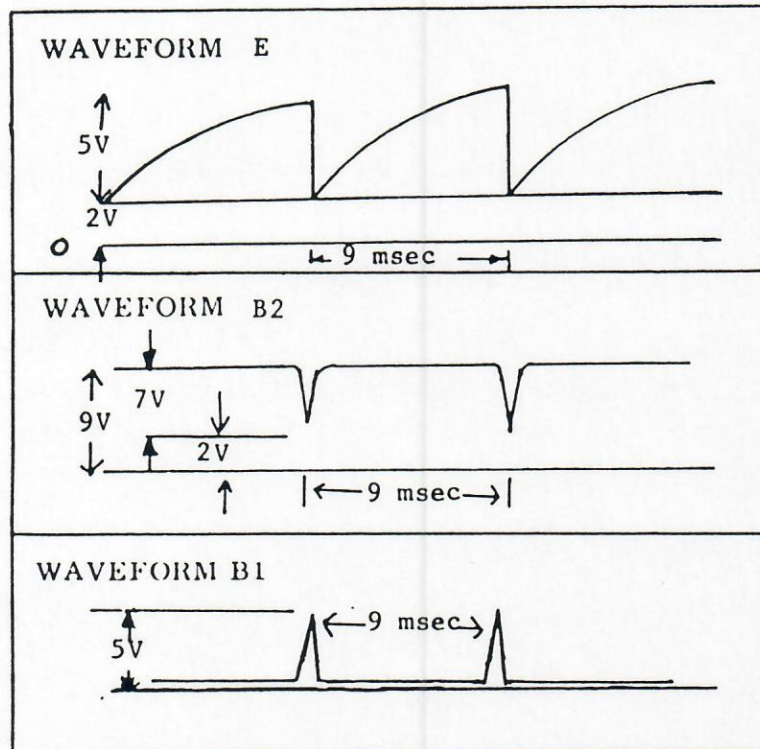
$$R_{BB} = \frac{(3.3K)V_{B2}}{(V1 - V_{B2})} = \frac{(3.3K)(6.5)}{(9.8 - 6.4)}$$

$$R_{BB} \approx 6.2K$$

UNIUNCTION SWEEP

An R - C network connected to the Emitter of the Unijunction Transistor is used to repetitively "Fire" the Unijunction. Each time the Unijunction fires the capacitor is discharged and must recharge to the firing voltage to repeat the cycle. The time constant of the R - C network determines the frequency of oscillation.

2. Waveforms



4. Measurement of Oscillation Period

PERIOD = 9 m sec

5. How does this time constant compare with the measured period?

Time Constant = 12.5 milliseconds

Period = 9 milliseconds

Note: The period of oscillation is not necessarily equal to the time constant of the R - C network. The Time Constant will, however, give the general order of magnitude of the Period.

In order to calculate the Period of the Unijunction Oscillator we must calculate the time required for the capacitor voltage to charge from zero to the firing voltage of the Unijunction.

UNIUNCTION SWEEP

From previous experiments we know that the Unijunction will fire at 4.8 volts.

$$\tau = 12.5 \text{ milliseconds}$$

$$V_c = V_{\text{source}} (1 - e^{-t/\tau}) = \text{Firing voltage}$$

$$V_c = 4.8 \text{ volts}, \quad V_{\text{source}} = 10 \text{ volts}$$

$$4.8 = 10(1 - e^{-t/12.5 \text{ msec}})$$

$$1 - e^{-t/12.5 \text{ m sec}} = 0.48$$

$$e^{-t/12.5 \text{ m sec}} = 0.52$$

$$\ln(e^{-t/12.5 \text{ m sec}}) = -\frac{t}{12.5 \text{ m sec}} = \ln(0.52) = -0.65$$

Note: Natural

Logarithm $-t = (-0.65)(12.5 \text{ m sec})$

$$t = 8.1 \text{ milliseconds}$$

Thus the period will be 9.1 milliseconds

$$P = 8.1 \text{ milliseconds}$$

This result agrees closely with the predicted value.

6. Minimum Series Resistance

$$R_{\min} = 90 \text{ K ohms}$$

7. Substitute a +10 MFD capacitor. What is the sweep period at a R = 100K setting?

$$\text{Period} = 2 \text{ sec}$$

Substitute a +100 MFD capacitor. What is the sweep period?

$$\text{Period} = 12 \text{ sec}$$

Add a +100 MFD cap in parallel (C = 200 MFD). What is the sweep period?

$$C = 200 \text{ MFD} - \text{Period} = 26 \text{ sec.}$$

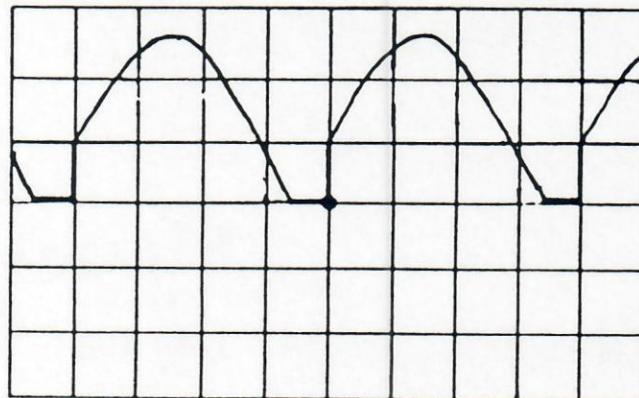
UNIUNCTION SCR CONTROL

This is a typical Industrial application of the Unijunction circuit driving an SCR power control circuit. Note that the Unijunction will fire at a set delay time after the commencement of each new A.C. cycle. The delay time is controlled by the setting of the 10K POT. When the unijunction fires, the voltage pulse from B1 will turn on the SCR and the current will flow in the LOAD. Note that the control circuitry is all low power and the only load current switching device is the SCR.

2. Data Table - Output Voltage

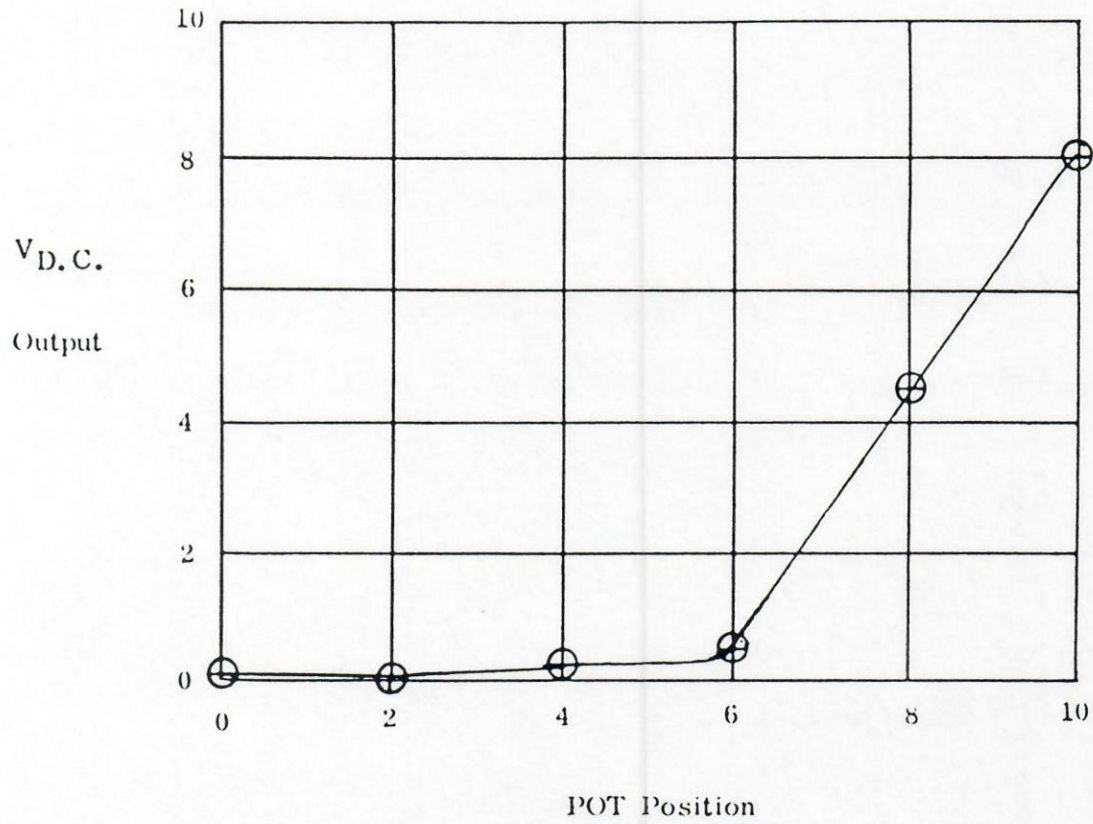
POT POSITION	D.C. VOLTAGE
0	0.0
2	0.0
4	0.1
6	0.5
8	4.6
10	8.0

4. Wave form



UNIJUNCTION SCR CONTROL

4. Output Voltage Versus POT POSITION



UNIJUNCTION DELAY-ON CONTROL

This circuit demonstrates the use of a Unijunction Transistor to generate a time delay before turning ON a load. When SWITCH A is placed UP the 100 μ fd capacitor begins to charge. When the Emitter voltage X reaches the firing voltage of the Unijunction the Unijunction will fire, turning ON the SCR. The amount of time delay is determined by the setting of the 100K POT.

3. Time Delay Data

POT POSITION	DELAY (seconds)
0	18 sec
2	13 sec
4	9 sec
6	6 sec
8	3 sec
10	1 sec

DIAC OPERATION

A STATIC or D.C. test of the DIAC is performed. The purpose is to note that the DIAC has a positive and negative "firing" voltage above which the resistance of the DIAC reduces dramatically. The DIAC is used in trigger circuits to assure a sharp and definite trigger point for an SCR or TRIAC. When the DIAC is in series with a TRIAC Gate, the breakdown or firing point of the DIAC provides a sudden surge of Gate current and voltage to turn the Gate ON.

2. Voltage Measurements

$V_{BR} = 7.6 \text{ VDC}$
$V_D = 0.7 \text{ VDC}$

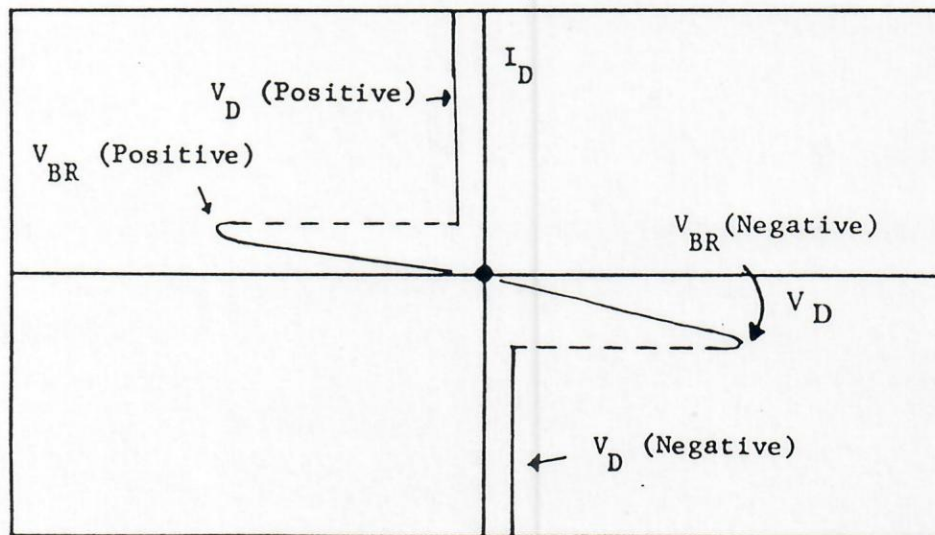
3. Reverse the meter leads and observe the same operation in the negative direction.

The operation is the same for negative voltages. The DIAC has no preferred polarity.

DIAC CHARACTERISTIC CURVE

The A.C. transformer is used to drive the DIAC circuit with positive and negative voltage. Current through the DIAC is displayed as the vertical deflection on the oscilloscope. The oscilloscope horizontal axis is the voltage across the DIAC. Note that the voltage scale is reversed because the oscilloscope common is connected to the intersection of the DIAC and the resistor.

2. Waveforms



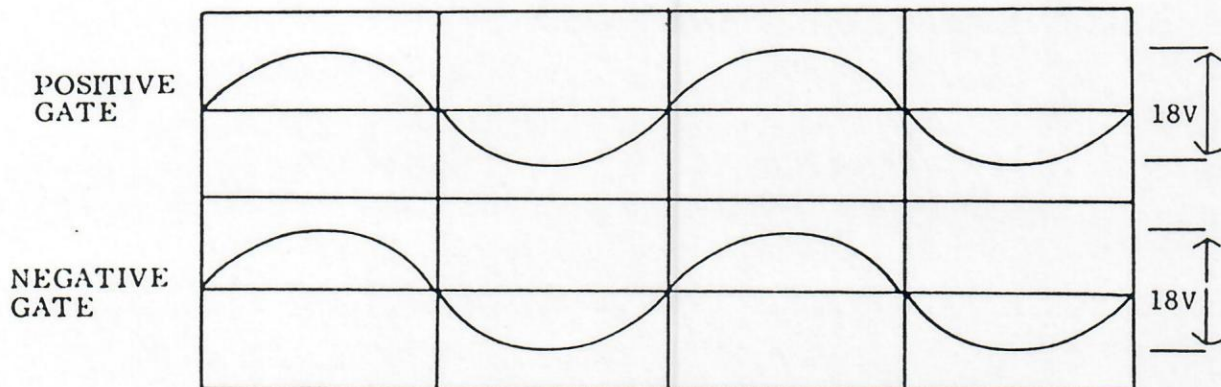
TRIAC OPERATION

This is a STATIC or D.C. test of the TRIAC. The low power Gate controls the high power Load for both positive and negative voltages. When the TRIAC turns ON it will be noted that the full A.C. wave is conducted by the TRIAC, whereas the SCR could only conduct half of the A.C. wave.

3. Measurement of "TURN ON" voltage.

$V_{T \text{ pos}}$	=	1.5 VDC
$V_{T \text{ neg}}$	=	1.5 VDC

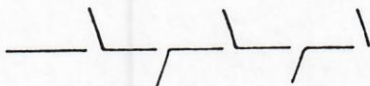
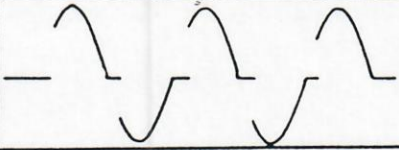
4. Waveforms



TRIAC PHASE SHIFT CONTROL

This is a practical TRIAC power control circuit. The output across the load is A.C. The Gate circuit is very similar to the one used in the SCR power control. This circuit is the type used in the Light Dimmers sold for home lighting control. Note that the power is controlled by switching the TRIAC ON and OFF not by dissipating the unused power in a resistor. This makes the circuit high in efficiency and a "Power Saving" device.

2. Waveforms

Lamp	Waveform
DIM	
MEDIUM	
BRIGHT	

TRIAC LATCHING AND HOLDING CURRENTS

The TRIAC will function properly only when a minimum load current is flowing in the circuit. The minimum load current required for the TRIAC to turn ON is called the LATCHING CURRENT. The minimum load current necessary for the TRIAC to remain ON is called the HOLDING CURRENT. This requirement for minimum load current explains why a TRIAC CONTROLLER does not operate over 100% of the A.C. Cycle. Typical specs will indicate that the TRIAC output can be controlled from 5% to 98% of the A.C. input wave.

3. TRIAC Voltage at the point where minimum HOLDING CURRENT is achieved.

$$V_H = 4 \text{ volts}$$

4. Calculation of HOLDING CURRENT

$$I_H = \frac{V_H}{2K} = \frac{4}{2K} = 2 \text{ ma}$$

$$I_H = 2 \text{ ma}$$

5. Measurement of TRIAC Voltage and Load Resistance at the point where the TRIAC is just able to turn ON.

$$R_L = 5K \text{ ohm}$$

$$V_L = 15 \text{ volts}$$

6. Calculation of LATCHING CURRENT

$$I_L = \frac{V_L}{R_V} = \frac{15}{5K} = 3.0 \text{ ma}$$

$$I_L = 3.0 \text{ ma}$$

DIGITAL ASTABLE MULTIVIBRATOR

The ASTABLE MULTIVIBRATOR is a basic oscillator circuit, commonly used where a square wave output is required. The frequency and the duty cycle are easily adjustable, making the circuit very versatile and popular.

3. Duty Cycle Measurement

POT POSITION	D.C. VOLTAGE	Estimate of Duty Cycle
0	1.6 V	25%
2	2.0 V	28.5%
4	2.2 V	33%
6	2.8 V	43%
8	3.8 V	58%
10	5.4 V	75%

INSTRUCTORS NOTE:

The student may be required to actually calculate the Duty Cycle using the formula given in the experiment.

Note that the D.C. voltage output is proportional to the Duty Cycle.

DIGITAL SERIES VOLTAGE CONTROL

This Voltage Control circuit provides pulsating power. The average voltage output is related to the Duty Cycle of the Astable Multivibrator. The main advantage to using this circuit is that the power is either ON or OFF. This results in very low power loss and good efficiency. The disadvantage of this circuit is that the power is constantly switching, generating switching noise transients and RFI. The output voltage requires considerable filtering to achieve low ripple D.C.

2. Output Voltage Variation.

CONTROL POT 100K (ASTABLE) POT	LAMP Brightness	D.C. VOLTAGE
0	VERY DIM	1.4 v
2	VERY DIM	1.6 v
4	BRIGHTER	2.0 v
6	MEDIUM	2.4 v
8	BRIGHTER	3.2 v
10	BRIGHT	4.5 v

PHOTOCELL SCR CONTROL

The PHOTOCELL is used as a component in an adjustable voltage divider which drives the Gate of an SCR. The Voltage Divider is adjusted so the Gate voltage is just below the turn on Threshold voltage of the SCR for ambient light conditions. Any reduction in the amount of light falling on the photocell will cause the photocell resistance to increase, causing an increase in the Gate voltage and turning the SCR ON. Note that the photocell carries very little current. The SCR controls the high Load Current.

3. Photocell Circuit Test

			Check
Step 1	ADJUST 1 MEG POT	LAMP OFF	✓
Step 2	HAND OVER Photocell	LAMP ON	✓

4. What is the furthest distance away from the photocell that you can place your hand to decrease the light enough to turn the lamp ON?

DISTANCE = 1 foot

Note that this circuit may be adjusted to be very sensitive to variations in light intensity. A circuit of this type may be used to dim the headlights on your car when another vehicle approaches.

STEP-UP TRANSFORMER

This is the introductory experiment to Transformers. The student will measure the STEP-UP Transformer input and output A.C. voltages and calculate the Turns Ratio.

2. Input and Output Voltages

set	measure		calculate
Switch A	$V_{\text{input A.C.}}$	$V_{\text{output A.C.}}$ (times 11)	Ratio = $\frac{V_{\text{output A.C.}}}{V_{\text{input A.C.}}}$
UP	38v p-p/13 VRMS	132v p-p/44 VRMS	3.47/ 3.38
DOWN	26v p-p/9.2 VRMS	165v p-p/57 VRMS	6.34/6.19

3. Calculate the Ratios and enter the results in the table. The Ratio for the SWITCH DOWN should be higher than that for the SWITCH UP position. Is this correct?

YES. Note that the Input Winding is indicated as being center tapped. This is verified in the calculated Ratio, differing by a factor of 2.

4. Loading Effects

R_{LOAD}	$V_{\text{AC OUTPUT}}$
33K	165Vp-p/55VRMS
10K	143v p-p/48.4 VRMS
3.3K	110V p-p/36 VRMS
1K	55V p-p/ 20.9 VRMS

Note that as the load is increased (smaller load resistor) the output voltage decreases.

AUTO-TRANSFORMER

A practical application of the Auto-Transformer is tested. The STEP-UP Ratio is measured. Note that the Auto-Transformer will offer the same A.C. STEP-UP performance as the multiple winding transformer but that it does not provide D.C. isolation between Input and Output.

2. Input and Output Voltage Measurement

V_{in} A.C.	= 11.5 VAC
V_{out} A.C.	= 26.5 VAC

3. Voltage Gain

$$GAIN = \frac{V_{out} \text{ A.C.}}{V_{in} \text{ A.C.}} = \frac{26.5}{11.5} = 2.3$$

Because the center tap is in the middle of the winding, the output has twice the windings compared to the input and the theoretical Gain should be 2. How does the measured Gain compare to this theoretical value?

The actual STEP-UP Ratio is 2.3. This is within the accuracy expected of this measurement.

4. Loading Effects

R_{LOAD}	$V_{AC \text{ out}}$
33K	27.0 VAC
10K	26.5 VAC
3.3K	25.5 VAC
1K	23.0 VAC

Note that the larger the load (smaller load resistance) the lower the output voltage.

RINGING - CHOKE CONVERTER/INVERTER

An Inverter is a device which generates A.C. output voltage from a D.C. Source. This type of system is used to generate A.C. power to operate appliances and Radio and T.V's aboard boats and in Recreational Vehicles where the basic power source is a battery. Note that the circuit consists of a D.C. driven oscillator which drives a STEP-UP transformer. The A.C. output is then rectified to provide D.C. output voltage at a different voltage level. This system is a Converter. This type of system is necessary when converting from one D.C. voltage to another because a Transformer will not work at D.C.

2. Inverter Output Voltage

$$V_{AC} = 50 \text{ VAC peak to peak}$$

3. Converter Output Voltage

$$V_{DC} = 10 \text{ VDC}$$

D.C. TO A.C. CONVERTER

This system is one of the type found in marine and recreational vehicle applications. The output of this type of system is not a true sine wave. The A.C. power output is useful for driving motors and lighting systems.

2. A.C. Output Voltage

$$\text{Output } V_{A.C.} = 19 \text{ VAC RMS}$$

3. Output Power

$$P_{\text{output}} = \frac{(V_{AC})^2}{R_L} = \frac{(19)^2}{15K} = 24 \text{ milliwatts}$$

4. Loading Effect

R_L	Output $V_{A.C.}$
100K	20 VAC RMS
56K	19.5 VAC RMS
15K	19.0 VAC RMS
10K	18.0 VAC RMS
1K	8.0 VAC RMS

5. Results using other base resistor.

Changing the value of the base resistor changes the frequency of oscillation of the Converter.

D.C. TO D.C. CONVERTER

The D.C. to A.C. Converter or Inverter circuit is used to drive a full wave rectifier bridge to generate D.C. This circuit is used to STEP-UP a D.C. voltage to a higher level.

2. Input and Output Voltages.

Input	$V_{D.C.}$	=	1.5 VDC
Output	$V_{D.C.}$	=	12 VDC

3. Ratio of Output to Input Voltage

RATIO	=	8
-------	---	---

TWO-TRANSFORMER INVERTER

Note that in the Two - Transformer Inverter there is a starting resistor connected to the base of the oscillator transistors. This resistor causes an unbalance in the quiescent point of the transistors and facilitates starting the oscillation. The 180° phase shift necessary for oscillation is provided by the left-hand transformer.

3. Peak to Peak Voltage Measurement

$$\text{OUTPUT } V_{AC} \text{ Rms} = \frac{(\text{A.C. Pk to Pk})}{2.8} = \frac{(80)}{2.8} = 28.5$$

4. Calculation of Output Power

$$P_{out} = \frac{(V_{AC})^2}{R} = \frac{(V_{AC})^2}{10K} = 81.5 \text{ milliwatts}$$

5. D.C. Input Voltage

$$\text{INPUT } V_P = 4.0 \text{ VDC}$$

6. Input Current Measurement

$$V_R = 2.5 \text{ VDC}$$

7. Input Current

$$I_P = 25 \text{ ma.}$$

8. Input Power

$$P_{in} = (25 \times 10^{-3})(4.0) = 100 \text{ milliwatt}$$

9. Power Conversion Efficiency

$$E = 81.5 \%$$

TRANSFORMER INDUCTANCE

The Inductive Reactance is measured for a Transformer Winding. The reactance is measured when the transformer is very lightly loaded (Unsaturated) and when a heavy load (100 ohm) is connected (Saturated). The heavy load causes large currents to flow in the windings, saturating the transformer core and causing the reactance to be reduced. In this experiment the coil resistance and the losses in the transformer core are neglected. The aim of this experiment is to show the student that when a reactor core is saturated, the inductive reactance decreases and Inductor presents a low impedance to A.C. current.

2. Measurement of A.C. and D.C. Voltages

set		measure		calculate	
Switch	Voltage	V_R	V_L	$I_L = \frac{V_R}{R} = \frac{V_R}{100}$	$\frac{V_L}{I_L}$
Switch A UP	D.C.	2.4	0.2	23 ma	$R_L = 8.3 \Omega$
Switch A DOWN	A.C.	1.2VAC	4.2	12 ma	$X_L = 350 \Omega$

4. How does the A.C. (Impedance (Z_L) and the D.C. Resistance (R_L) compare?

The A.C. Reactance is much higher than the D.C. Resistance.

5.

$$L = 931 \text{ mhy}$$

6. Saturated Reactor Voltage Measurements

Switch B UP (Load)

measure		calculate		
V_R	V_L	$I_L = \frac{V_R}{R} = V_R \times 10 \text{ ma}$	$ X_L = \frac{V_L}{I_L}$	$L_S = 2.66 X_L \text{ mhy}$ SATURATED
2.0 v	0.5	20 ma	25 ohm	$L_S = 66.5 \text{ mhy}$

TRANSFORMER	$L = 931 \text{ mhy}$
SATURATED	$L = 66.5 \text{ mhy}$

A.C. MAGNETIC AMPLIFIER

The Magnetic Amplifier is a device used where high reliability and ruggedness is required. It requires no semiconductors in the actual amplifier and is purely mechanical in construction, making it suitable for use in extreme environments.

3. Measurement of Input and Output Voltages

	CONTROL CIRCUIT		LOAD CIRCUIT		
Load	$V_{C(D.C.)}$	$V_R(D.C.)$	$V_{in(A.C.)}$	$V_{Load(A.C.)}$	$V_R(A.C.)$
DIM	1.9 VDC	0.5 VDC	13 VRMS	6.0 VRMS	2.3 VRMS
BRIGHT	4.8 VDC	1.2 VDC	12.5 VRMS	10 VRMS	3 VRMS

4. Calculation of Amplifier Currents and Power

	LOAD	DIM (1)	BRIGHT (2)
CONTROL CIRCUIT (D.C.)	$I_{D.C.} = V_{R D.C.} \times 10 \text{ ma}$	= 5 ma	= 12 ma
	$P_{D.C.} = I_{D.C.} \times V_C(D.C.)$	$P_{D.C. 1}$ = 9.5 mw	$P_{D.C. 2}$ = 57.6 mw
LOAD CIRCUIT (A.C.)	$I_{A.C.} = V_{R(A.C.)} \times 10 \text{ ma}$	= 23 ma	= 30 ma
	$P_{LOAD} = V_{LOAD A.C.} \times I_{A.C.}$	$P_{LOAD 1}$ = 138 mw	$P_{LOAD 2}$ = 300 mw
	$P_{in} = V_{in A.C.} \times I_{A.C.}$	$P_{in 1}$ = 299 mw	$P_{in 2}$ = 375 mw

A.C. MAGNETIC AMPLIFIER

5. Power Gain Calculation

$$P.G._1 = \frac{P_{Load\ 1}}{P_{D.C.\ 1}} = \frac{138\ \text{mw}}{9.5\ \text{mw}} = 14.5$$

$$P.G._2 = \frac{P_{Load\ 2}}{P_{D.C.\ 2}} = \frac{300\ \text{mw}}{57.6\ \text{mw}} = 5.2$$

How does this Power Gain for a Magnetic Amplifier compare to a Transistor or SCR circuit Power Gain? Why is Power Gain important?

Transistor circuit power gain can be in the order of 1000. The SCR power gain can be even higher. The magnetic amplifier has a more modest Power Gain, approximately 10. Power Gain is important because it defines the ability of a circuit to increase the driving capability or the ability to do work, of an input signal.

Efficiency Calculation

$$E_1 = \frac{P_{Load\ 1} \times 100\%}{P_{in\ 1} + P_{D.C.\ 1}} = \frac{138\ \text{mw}}{299\ \text{mw} + 9.5\ \text{mw}} = \frac{138}{308.5} = 44\%$$

$$E_2 = \frac{P_{Load\ 2} \times 100\%}{P_{in\ 2} + P_{D.C.\ 2}} = \frac{300}{375 + 57.6} = \frac{300}{427.6} = 69\%$$

E_1	44%
E_2	69%

Why is Efficiency important?

Efficiency represents the percentage of the total power input to a device that is delivered to the load. High efficiency is desirable because it means that less power is wasted by the circuit. This means that the power drain of the circuit will be low, allowing smaller devices, less power input, lower cost to manufacturer and lower cost to operate.

D.C. MAGNETIC AMPLIFIER

The D.C. Magnetic Amplifier consists of an A.C. Magnetic Amplifier with the A.C. output voltage rectified by a full wave bridge rectifier. Note that the Magnetic Amplifier cannot work with a D.C. V_{in} because the D.C. current will not be affected by the change of inductance in the transformers.

2. Measurement of Circuit Voltages

Load	Control Input		Load Circuit		
	V_{in} D.C.	$V_{R INPUT}$	V_{in} A.C.	V_R D.C.	V_{LOAD} D.C.
MED. BRIGHT	4 VDC	1 VDC	12.5 VRMS	2.6 V	8 VDC

3. Power Calculations

CONTROL	$I_{D.C.} = V_{R INPUT} \times 10 \text{ ma}$	$I_{D.C.}$ = 10 ma
	$P_{D.C.} = I_{D.C.} \times V_{in D.C.}$	$P_{D.C.}$ = 40 mw
LOAD	$I_{LOAD} = V_{R D.C.} \times 10 \text{ ma}$	I_{LOAD} = 26 ma
	$P_{LOAD} = V_{LOAD} \times I_{LOAD}$	P_{LOAD} = 208 mw
	$P_{INPUT} = V_{in A.C.} \times I_{Load}$	$P_{INPUT A.C.}$ = 325 mw

D.C. MAGNETIC AMPLIFIER

4. Power Gain and Efficiency Calculations

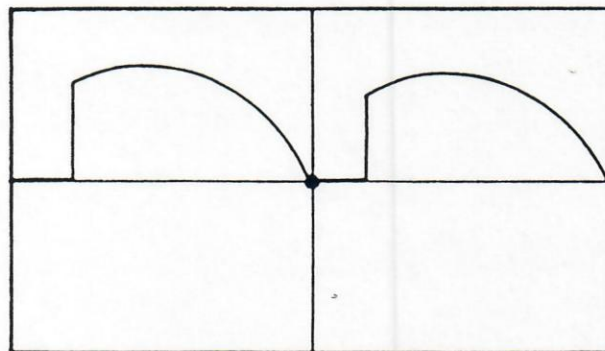
$$\text{Power Gain} = \frac{P_{\text{Load}}}{P_{\text{D.C. Control}}} = \frac{208 \text{ mw}}{40 \text{ mw}} = 5.2$$

$$\text{Efficiency} = \frac{P_{\text{Load}}}{(P_{\text{in}} + P_{\text{CONTROL}})} = \frac{208 \text{ mw}}{(40 + 324) \text{ mw}} = 56\%$$

FULL WAVE SCR BRIDGE

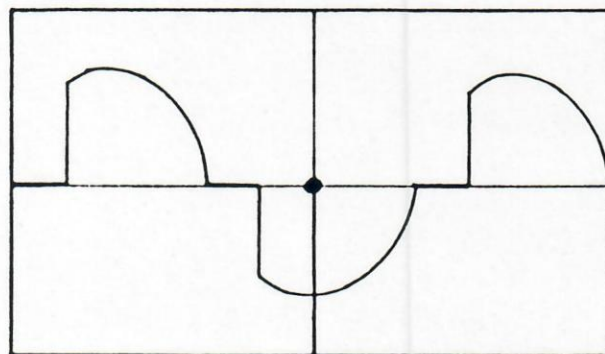
The Full Wave SCR Bridge is used to control Full Wave A.C. current to an A.C. load. Note that this is a high efficiency circuit and that the control circuit is isolated from the Power Circuit (bridge) by a transformer, providing protection of the control components. The power necessary to regulate the A.C. load power is very small.

2. Waveform D.C.



D.C. LOAD VOLTAGE

3. Waveform A.C.



A.C. LOAD VOLTAGE

Note: One major feature of SCR power control circuits is that the power control does not waste the unused power. During the unused portion of the power output cycle the circuit is OFF and the power is simply unused.



Ed-Lab
ANSWER MANUAL

TRANSISTORS

6

UNIT NO.
CES INDUSTRIES, INC.

NPN TRANSISTOR

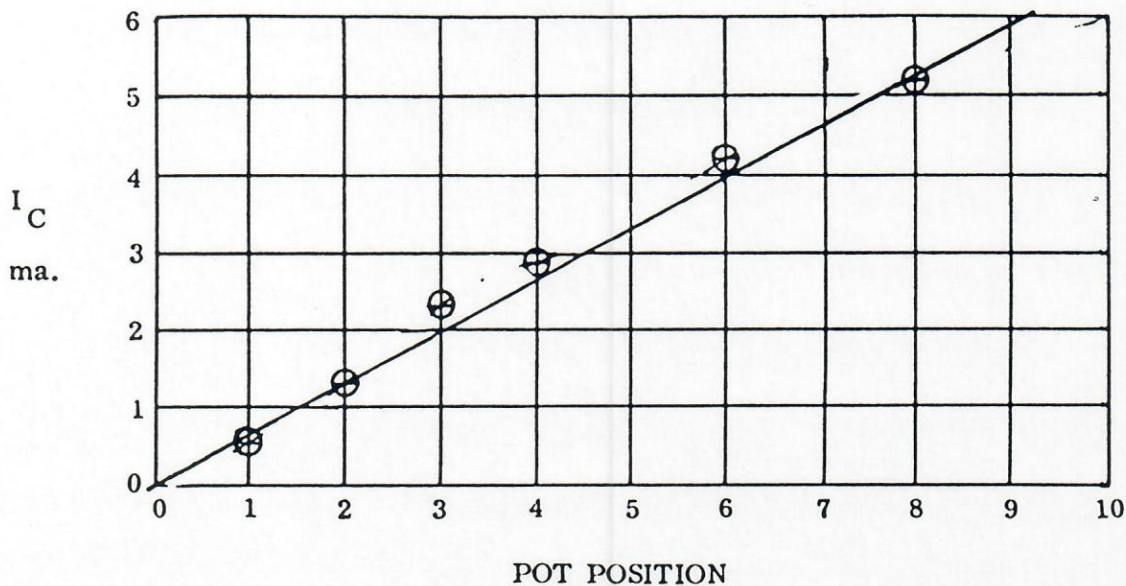
The purpose of this experiment is to perform a static or D.C. test of an NPN transistor. The base voltage is varied and the base, collector and emitter voltages and currents are measured. The measurements are used to calculate the Current Gain (Beta) and the Alpha of the transistor.

1. The current is found for the base collector and emitter by measuring the voltage across the base, collector and emitter resistors and then using OHM'S LAW to calculate the current.
2. Note that the lamp will be dim throughout this experiment because there is a 1K resistor in series with the lamp. Voltages across the Base Resistor, Emitter Resistor and Collector Resistor are measured and then the Base, Emitter and Collector currents are calculated.

SET	READ			CALCULATE (see examples)		
POT POSITION	V_{BR}	V_{ER} (left)	V_{CR} (right)	$I_B = \frac{V_{BR}}{100K}$ (÷ 100 ma)	$I_E = \frac{V_{ER}}{100}$ (x10 ma)	$I_C = \frac{V_{CR}}{1000}$ (x 1 ma)
0	0	0	0	0	0	0
1	0.5	0	0.5	0.005	0	0.5
2	1.4	0.1	1.2	0.014	1	1.2
3	2.25	0.19	2.2	0.0225	1.9	2.2
4	3.0	0.26	2.9	0.03	2.6	2.9
6	4.25	0.4	4.1	0.0425	4	4.1
8	5.8	0.45	5.2	0.058	4.5	5.2
10	7.0	0.6	6.0	0.07	6	6.0

NPN TRANSISTOR

4. The Emitter and Collector Currents are nearly the same. The emitter current should be slightly larger because the current in the emitter is equal to the current in the collector plus the current flowing in the base. While the base current is small, it is still measureable.
5. The collector current is proportional to the base current and much larger in size.
6. This is a plot of the POT POSITION versus the COLLECTOR CURRENT in ma. Since the POT POSITION is proportional to base voltage and the base current is proportional to the voltage, then the collector current should be proportional to the POT POSITION.



7. The current will level off at high base input (high POT position) because the transistor will saturate. Saturation means that the Collector-Emitter voltage of the transistor will approach zero and the transistor will no longer be able to cause a change in the collector or emitter circuit.
9. Calculation of Beta

$$\text{Transistor Beta} = \frac{I_C}{I_B}$$

Using the calculated current data from the Table for POT POSITION 3 we find that:

$$I_B = 0.0225 \text{ ma}$$

$$I_C = 2.2 \text{ ma}$$

$B = \frac{2.2}{0.0225} = 97.8$

NPN TRANSISTOR

10. Calculation of Alpha

Alpha is the ratio of the collector to the emitter current.

$$\text{ALPHA} = \frac{I_C}{I_E}$$

Since I_C and I_E are nearly the same, it is inaccurate to use the measured values of I_C and I_E to find the Alpha. If we use the measured value of I_C or I_E and the measured value of I_B we will get a much more accurate answer.

KIRCHHOFF'S CURRENT LAW for the transistor says:

$$I_E = I_B + I_C \quad (\text{The current in the emitter is the current in the collector plus the current in the base})$$

$$\text{ALPHA} = \frac{I_C}{I_E} = \frac{I_E - I_B}{I_E} = 1 - \frac{(I_B)}{(I_E)}$$

Using the values from the table for POT POSITION 3 we get:

$$I_B = 0.0225 \text{ ma}$$

$$I_E = 1.9 \text{ ma}$$

$$\text{ALPHA} = 1 - \frac{(I_B)}{(I_E)} = 1 - \frac{0.0225}{1.9} = 0.988$$

11. If the transistor Beta is 50 and the Collector Current is 0.25 amperes, what is the Base Current?

$$\beta = 50$$

$$I_C = 0.25 \text{ a}$$

$$I_B = ?$$

$$\beta = \frac{I_C}{I_B} \therefore I_B = \frac{I_C}{\beta} = \frac{0.25}{50} = 0.005 = 5 \text{ ma}$$

13. Operation of a Transistor.

The transistor is a device with three terminals, called the Collector, Base and Emitter. The current flowing into the base of the transistor controls the Collector and emitter current that will flow in the transistor. The Collector Current is Beta times the Base Current. The Emitter Current is the Collector Current plus the Base Current, obeying Kirchhoff's Current Law.

COMMON EMITTER D.C. AMPLIFIER

The circuit is a Common Emitter Amplifier with a variable voltage connected to the base circuit. Output voltage is measured at the transistor collector. The student will take data on the output voltage at the collector versus the input voltage to the base circuit and the results will be plotted. Amplifier Gain and Transistor Current Gain are calculated.

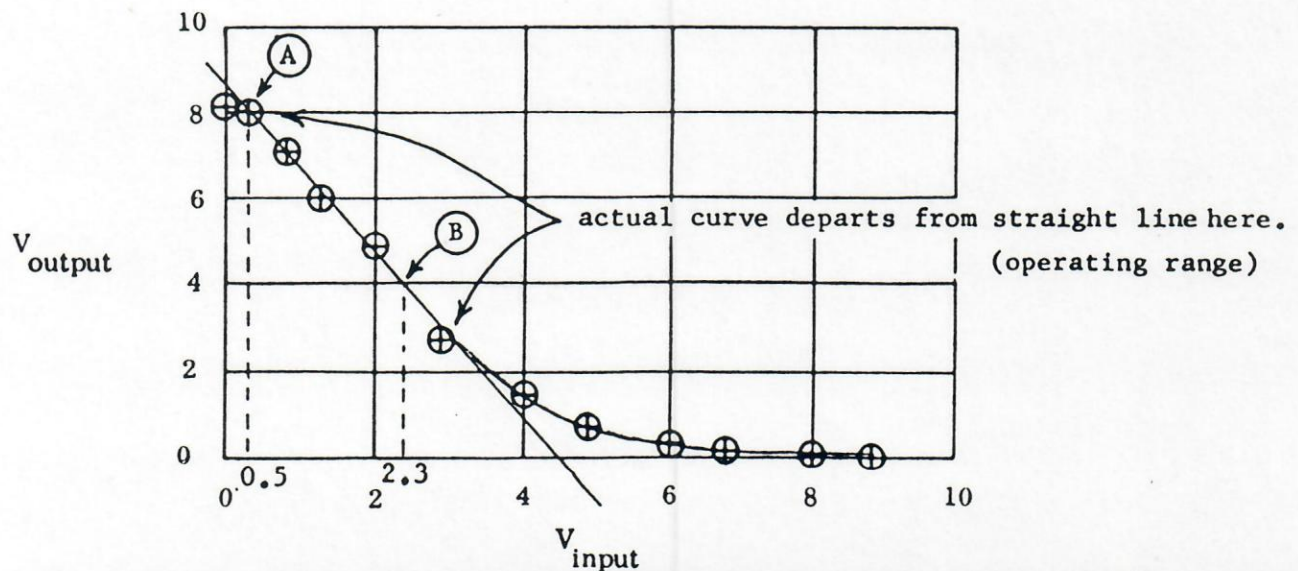
3. Data Table - Input Voltage and Output Voltage

Switch A Down	Switch A UP
V_{input}	V_{output}
0 volts	8.2
1	6.6
2	4.8
3	3
4	1.5
5	0.4
6	0.1
7	0
8	0

Note: The V_{output} data will vary between reports because of the difference in the BETA of individual transistors.

4. Input - Output Graph

The results of the data in the table of paragraph 3 are plotted on a graph.



COMMON EMITTER D.C. AMPLIFIER

- (b) The straight line drawn on the graph connecting points A and B is the line indicating the linear portion of the gain curve. Points A & B are selected as the points to use in the calculation of the amplifier gain.

$$\text{GAIN} = \frac{V_{\text{out B}} - V_{\text{out A}}}{V_{\text{in B}} - V_{\text{in A}}} = \frac{8 - 4}{0.3 - 2.3} = \frac{4}{-2.0} = -2$$

5. The linear operating range of the amplifier is the portion of the Input-Output Curve which conforms to the straight line drawn through A and B.

INPUT VOLTAGE OPERATING RANGE		
V_{input} MINIMUM	=	0.3 volts
V_{input} MAXIMUM	=	3.5 volts
Range (MAX-MIN)	=	3.5 - 0.3 = 3.2 volts

6. Transistor Gain Calculation

Following the diviation given in the experiment

$$\beta = (G) \frac{R_B}{R_C} = 2 \left(\frac{56}{1} \right) = 112$$

$$\beta = 112$$

7. Amplifier Gain Calculation for any size Base and Collector Resistors.

Since $\text{GAIN} = -\beta \frac{R_C}{R_B}$ we can substitute the resistor values of $R_C = 2.2K$ and $R_B = 100K$

and using the value of Beta found in paragraph 6 of 112 the amplifier gain should be:

$$\text{Gain} = -112 \frac{(2.2)}{(100)} = -2.46$$

8. The Common Emitter Amplifier is constructed using the resistor values given in step 7 and the gain is measured by using two points in the linear portion of the curve as was done in step 4.

COMMON EMITTER D.C. AMPLIFIER

	set	read
POINT	Switch A UP	Switch A DOWN
	V_{output}	V_{input}
A	2	$V_A = 3.3 \text{ volts}$
B	6	$V_B = 1.5 \text{ volts}$

The gain is calculated as:

$$K = - 2.22 \quad K = \frac{(V_{\text{out B}} - V_{\text{out A}})}{(V_{\text{in B}} - V_{\text{in A}})} = \frac{6 - 2}{1.5 - 3.3} = \frac{4}{1.8} = -2.22$$

9. The measured gain and the theoretical gain compare as follows:

Theoretical Gain (Paragraph 7) = - 2.46

Measured Gain (Paragraph 8) = - 2.22

The percent difference is:

$$\frac{\text{Gain Theoretical} - \text{Gain Measured}}{\text{Gain Theoretical}} \times 100 = \frac{2.46 - 2.22}{2.46} \times 100 = 9.7\%$$

10. For

$$B = 80$$

$$R_B = 100K$$

$$R_C = 3.3K$$

$$\text{GAIN} = \beta \frac{R_C}{R_B} = 80 \frac{(3.3)}{(100)} = 2.64$$

COMMON EMITTER D.C. AMPLIFIER

11. Comparison of Beta found in experiment No. 1 and in experiment No. 2.

Beta from experiment No. 1 = 97.8

Beta from experiment No. 2 = 112

These values are in acceptable agreement.

TRANSISTOR BETA TESTER

A transistor is connected in a collector biased or self biased circuit so the transistor is in its linear region. The Beta of the transistor is calculated from the Collector output voltage. The base resistor must be selected so that the transistor collector voltage is about half of the supply voltage. This assures that the transistor will be operating in the middle of its linear region of operation. The derivation of the formula for the transistor Beta is given in the experiment description.

2.

data				
TRANSISTOR	V_C	R_B	+V1	CALCULATE BETA
Q4	7.0	470K	8.8	96.1
Q5	6.4	470K	8.8	128.2
Q6	7.9	470K	8.9	52.8
Q7	3.4	470K	8.6	60.5

Note: The beta of the particular transistors in each students Ed-Lab 650 trainer will be somewhat different from these values.

COMMON EMITTER AMPLIFIER BIASING

In this experiment various methods of biasing transistors will be investigated. The advantages and disadvantages of each method will be noted. The stability of the different bias circuits will be studied. A stable bias system is one which will be relatively independent of the transistor Beta, making it useful for many different transistors.

1. Each bias network is tested with a variety of transistors. The more stable circuits will have the least change in Collector Voltage for different transistors.

Figure	Circuit	TRANSISTOR Q5		V _C (STABILITY)		
		V _C (output)	R _B (estimated)	Q4	Q6	Q7
4 - 1	Small Signal Bias	5 v	2 M	5.5	6.8	5.0
4 - 2	Emitter Bias	3.4	470K	4.2	4.8	2.8
4 - 3	Voltage Divider Bias	4.0	100K	4.0	4.4	7.5
4 - 4	Collector Feedback Bias	5.0	1.2 M	5.2	6.2	5.8

A.C. COMMON EMITTER AMPLIFIER

The A.C. Common Emitter Amplifier circuit is built and tested. The student learns to adjust the bias of an amplifier circuit for the correct collector output voltage. He also must adjust the input signal amplitude to prevent clipping and saturation of the transistor. The voltage gain of the circuit is measured.

2. Input and Output Voltage Measurements.

$$V_A = 0.9 \text{ volts peak to peak}$$

$$V_{in} = 0.009 \text{ volts peak to peak}$$

$$V_{out} = 1 \text{ volt peak to peak}$$

4. Calculation of amplifier GAIN, G.

$$G = \frac{V_{out}}{V_{in}} = \frac{1}{0.009} = 111$$

Note: Any distortion of the output waveshape may be caused by the 100 ufd A.C. coupling capacitor as well as the transistor amplifier. The bias must be adjusted to prevent clipping or saturation of the transistor.

COMMON EMITTER INPUT AND OUTPUT IMPEDANCE

The Input and Output Impedance of a Common Emitter Amplifier are measured. The technique used is to find the load which causes the voltage to be half the value of the unloaded signal. This load is then equal to the impedance of the circuit. The student should realize that this technique is a general one and can be used on most circuits.

4.

1.	V_{out} A.C. $(R_m = 0)$	<u>NORMAL VOLTAGE</u> $V_{out} = \frac{2 \text{ volts}}{\text{peak to peak}}$
2.	Adjust R_m for $1/2 V_{out}$ $(1/2 V_{out} = 1 \text{ v p-p})$	<u>INPUT IMPEDANCE</u> $R_m = R_{in} = 2K \text{ ohm}$
3.	Remove R_m . Add R_L . Adjust R_L for $1/2 V_{out}$	<u>OUTPUT IMPEDANCE</u> $R_L = R_{out} = 5K \text{ ohm}$

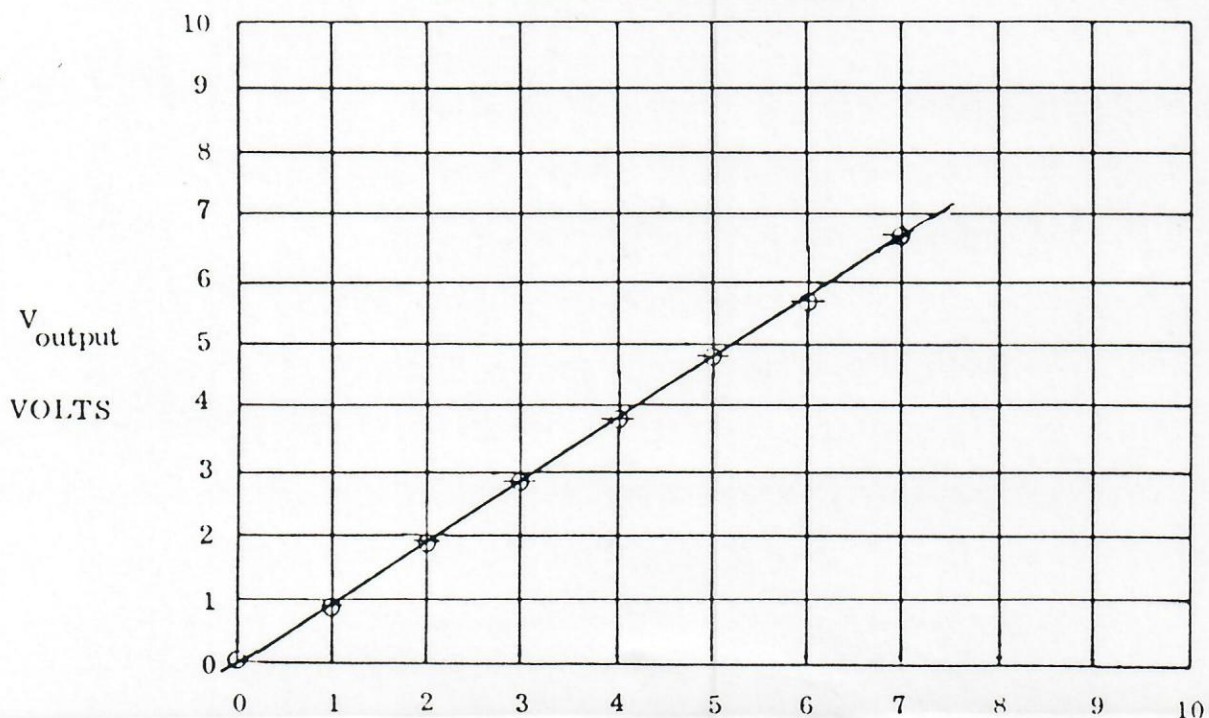
COMMON COLLECTOR AMPLIFIER OR EMITTER FOLLOWER

The Common Collector or Emitter Follower circuit is built and tested. The basic characteristics of the Emitter Follower circuit are Unity Gain and High Input Impedance.

2.

SWITCH A DOWN	SWITCH A UP
V_{input} VOLTS	V_{output} VOLTS
0	0
1	0.9
2	1.9
3	2.85
4	3.8
5	4.8
6	5.8
7	6.7
8	7.7
9	---

3.



COMMON COLLECTOR AMPLIFIER OR EMITTER FOLLOWER

4. Calculation of the GAIN of the Common Collector Amplifier.

$$\text{GAIN} = \frac{(V_{\text{outA}} - V_{\text{outB}})}{(V_{\text{inA}} - V_{\text{inB}})} = \frac{7.7 - 0}{8 - 0} = 0.96$$

GAIN = 0.96

5. The gain of the Emitter Follower circuit is slightly less than 1.
6. Input Voltage versus output voltage for various combinations of base and emitter resistors.

R_B	R_E	V_{out}
3.3K	3.3K	5.0
3.3K	2.2K	4.9
10K	2.2K	4.8
0 (shorted)	3.3K	5.0
1K	1K	4.8
100K	4.7K	4.0
1M	33K	4.1

Note: V_{input} is kept constant while R_E and R_B are varied.

7. Comment on the variation in V_{out} for different R_B and R_E resistors.

The V_{out} remains relatively constant for various combinations of Base and Emitter resistances. The high input impedance at the amplifier base makes the circuit fairly insensitive to changes in drive impedance and load impedance.

8. Why is this circuit called an EMITTER FOLLOWER?

The circuit is called an Emitter Follower because the Output Voltage at the Emitter follows the Input Voltage.

E. F. INPUT AND OUTPUT IMPEDANCE

The Input and Output Impedance of the Emitter follower circuit are measured using the technique of loading the input and output circuits until the voltage is half the unloaded value. The load used is then equal to the circuit impedance. Note that the circuit has a very high input impedance and a very low output impedance. This makes the Emitter Follower circuit suitable as a buffer where a high impedance source is used to drive a low impedance load.

2. Output Voltage

$$V_{\text{out}} = 5.8 \text{ volts}$$

3. The output is loaded with the 1K POT until the output voltage is half the value in step 3 or 2.9 volts.

$$1/2 V_{\text{out}} = 2.9 \text{ volts}$$

$$R_{\text{output}} = 50 \text{ ohms approx.}$$

4. The Base resistor is increased until half voltage output is achieved.

$$R_{\text{input}} = 280K \text{ ohm approx.}$$

EMITTER BIAS DEGENERATION

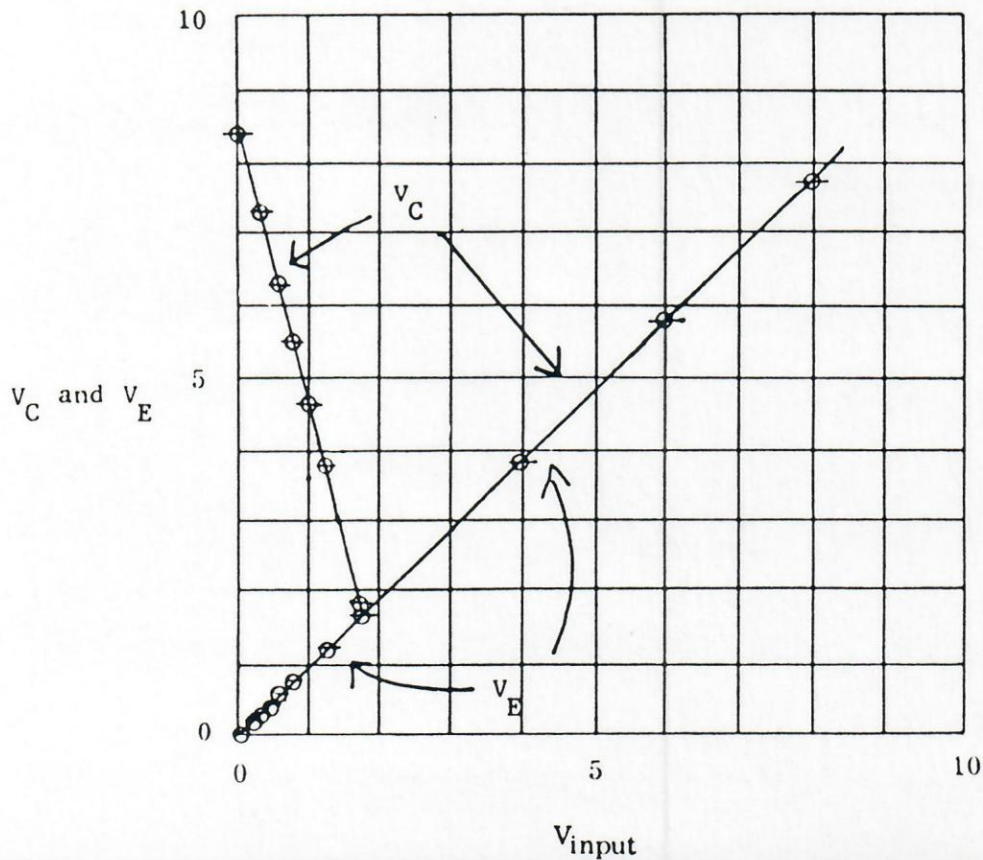
The operation of a transistor amplifier with an emitter resistor is studied. The emitter resistor causes a decrease in gain of the amplifier below the gain of a Common Emitter Amplifier. This decrease in gain can be looked at as negative feedback. The advantage of including an emitter resistor in an amplifier is that it stabilizes the D.C. bias point of the amplifier.

2. Table of Emitter Voltage and Collector Voltage versus Input Voltage.

V_{in}	V_E	V_C
0	0	8.2
.2	0.16	7.4
.4	0.32	6.3
.6	0.55	5.5
.8	0.70	4.75
1	0.90	3.90

V_{in}	V_E	V_C
1.5	1.3	1.7
2	1.8	1.8
4	3.8	3.8
6	5.8	5.8
8	7.8	7.8
9	—	—

3. Graph of results of table in step 2.



EMITTER BIAS DEGENERATION

4. Calculation of GAIN.

$$\text{COLLECTOR GAIN} = \frac{\Delta V_C}{\Delta V_{in}} = \frac{-4.3}{1} = -4.3$$

$$\text{EMITTER GAIN} = \frac{\Delta V_E}{\Delta V_{in}} = \frac{+7.8}{8} = 0.975$$

The gain is very close to the theoretical value. If we neglect the collector resistor, the circuit is an Emitter Follower, therefore the Emitter Gain of 0.975 agrees with the expected gain of an Emitter Follower Circuit. The theoretical Collector Gain is 4.7.

$$\% \text{ Error} = \frac{4.7 - 4.3}{4.3} \times 100 = 9\%$$

5. What is the linear operating range for the input voltage?

The transistor is operating in the linear region for input voltages of 0 to 1.5 volts. This is seen on the graph of step 3 as the range of input voltages over which the Collector voltage exhibits a linear variation.

6. What is the linear operating range for the collector output voltage?

The linear operating range of the Collector Voltage is 8.2 to 1.8 volts. This is the region seen in the graph of step 3 where the Collector Voltage variation is a straight line.

7. What BIAS point should you select?

The correct Bias Point is the point where the collector voltage is in the middle of its linear range.

$$\text{BIAS POINT} = \frac{8.2 - 1.8}{2} + 1.8 = 5 \text{ volts}$$

8. What component would you change and what value would you substitute to obtain a gain of 10?

In order to change the GAIN to 10 we must change R_C and R_E such that:

$$\text{GAIN} = \frac{R_C}{R_E} = 10 \quad \text{WITH AN } R_C \text{ of } 4.7K \quad 10 = \frac{4.7K}{R_E}$$

$$R_E = \frac{4.7K}{10} = 470 \text{ ohms}$$

EMITTER BIAS DEGENERATION

WITH AN R_E of 1K

$$10 = \frac{R_C}{1K}$$

$R_C = 10K$

Any set of resistor values which satisfy the given equation equal to 10 can be used.

EMITTER BYPASS CAPACITOR

An Emitter Bypass Capacitor is added across the Emitter Resistor of a transistor amplifier. This capacitor is a very low impedance at the signal frequency, effectively shorting the emitter resistor for the A.C. signal. This allows the circuit to have the D.C. bias stability of the Emitter Bias circuit shown in Experiment #9 with the signal gain of the Common Emitter circuit of Experiment #5.

2. Input and Output Voltage Measurements.

$$\text{A.C. } V_{in} \text{ (Point A)} = 0.5 \text{ volts p-p}$$

$$\text{A.C. } V_{out} \text{ (Collector)} = 2.4 \text{ volts p-p}$$

3. GAIN Calculation

$$\text{GAIN} = \frac{\text{A.C. } V_{out}}{\text{A.C. } V_{in}} = \frac{2.4}{0.5} = 4.8$$

8. Input and Output Voltage Measurement.

$$\text{A.C. } V_{output} = 5.4 \text{ volts p-p}$$

$$\text{A.C. } V_{input} \text{ at point A} = 5 \text{ volts p-p}$$

9. GAIN Calculation

$$\text{Gain} = \frac{\text{A.C. } V_{output}}{\text{A.C. } V_{input} \text{ at B}} = \frac{5.4}{0.05} = 108$$

$$\text{GAIN} = 108$$

10. What is the function of the By-Pass Capacitor?

The By-Pass Capacitor causes the A.C. signal to bypass the emitter resistor and avoid emitter degeneration. This makes the circuit A.C. GAIN high, while preserving the bias point stability of the emitter resistor.

EMITTER BYPASS CAPACITOR

11. How does the high gain calculated above using the By-Pass Capacitor compare with the Common Emitter Amplifier Gain measured in Experiment No. 5?

The gain of the Common Emitter Amplifier (Experiment 34) and the Emitter By-Pass Capacitor Amplifier are nearly the same. The reason for this, is that for A.C. signals, the emitter resistor is shorted and the circuits are nearly identical.

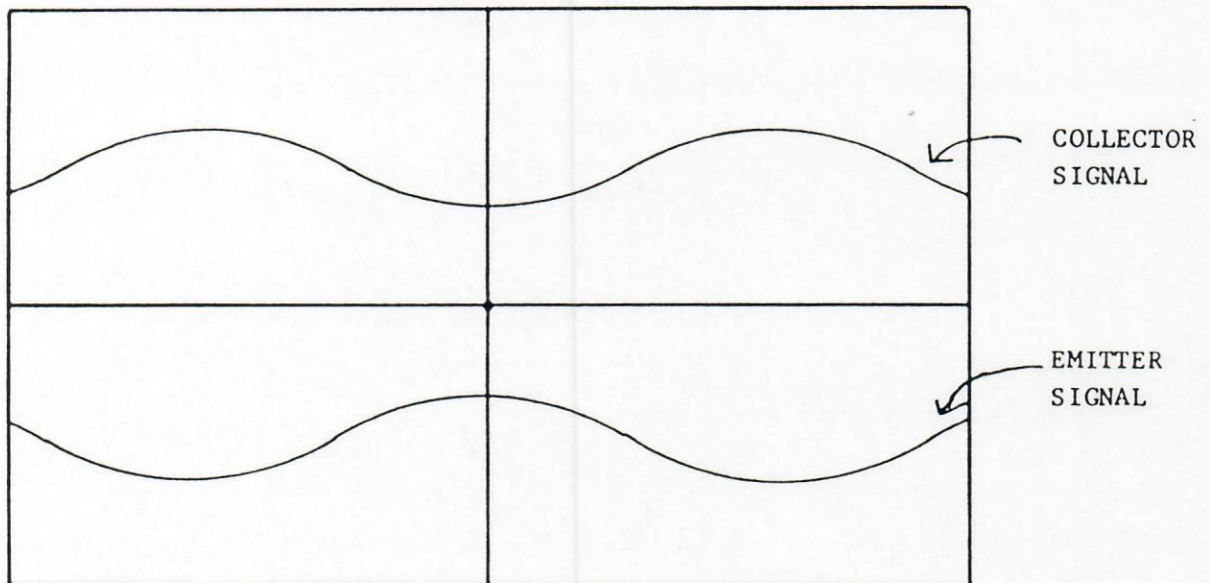
DYNAMIC AMPLIFIER & PHASE SPLITTER

A transistor with a Collector and an Emitter resistor is used as a Phase Splitter. The output from the collector and the output from the emitter are 180° out of phase. These two signals are alternately displayed on the oscilloscope as the transistor switch Q5 is turned ON and OFF by the square wave output of the signal generator. Note that the Collector signal will always be more positive than the emitter signal, so when Q5 is ON, D5 is reverse biased and the Collector signal will be displayed. When Q5 is OFF the Emitter signal will be displayed.

2. The bias must be adjusted to avoid clipping and saturation. In the linear region of operation the waveforms are 180° out of phase.

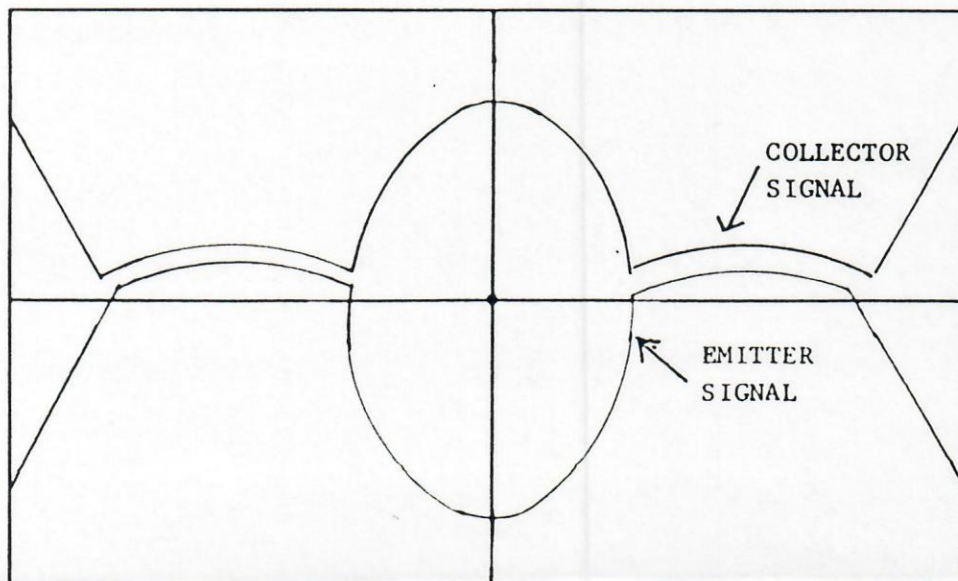
3. Output Waveforms

UNDISTORTED SIGNAL OUTPUT



4.

DISTORTED SIGNAL OUTPUT



DYNAMIC AMPLIFIER & PHASE SPLITTER

5. What is the maximum undistorted collector output A.C. signal voltage? What is the maximum permitted input A.C. voltage for an undistorted output?

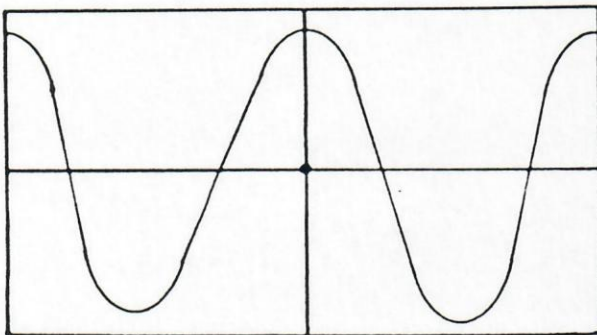
The maximum output voltage for undistorted operation is 1.7 volts peak to peak.
The maximum input voltage is 2 volts peak to peak.

6. What is the PHASE RELATIONSHIP between the collector output (C) and the emitter output (E)?

The Collector Waveform is 180° out of phase with the Emitter Waveform.

7. Vary the amount of "emitter by-pass" using the 1K POT. What is the effect on the amplifier GAIN and BIAS? Sketch the undistorted high gain output below:

As the 1K POT is adjusted so that the Emitter By-Pass Capacitor bypasses more of the emitter resistance the Collector Output increases and the Emitter output decreases.

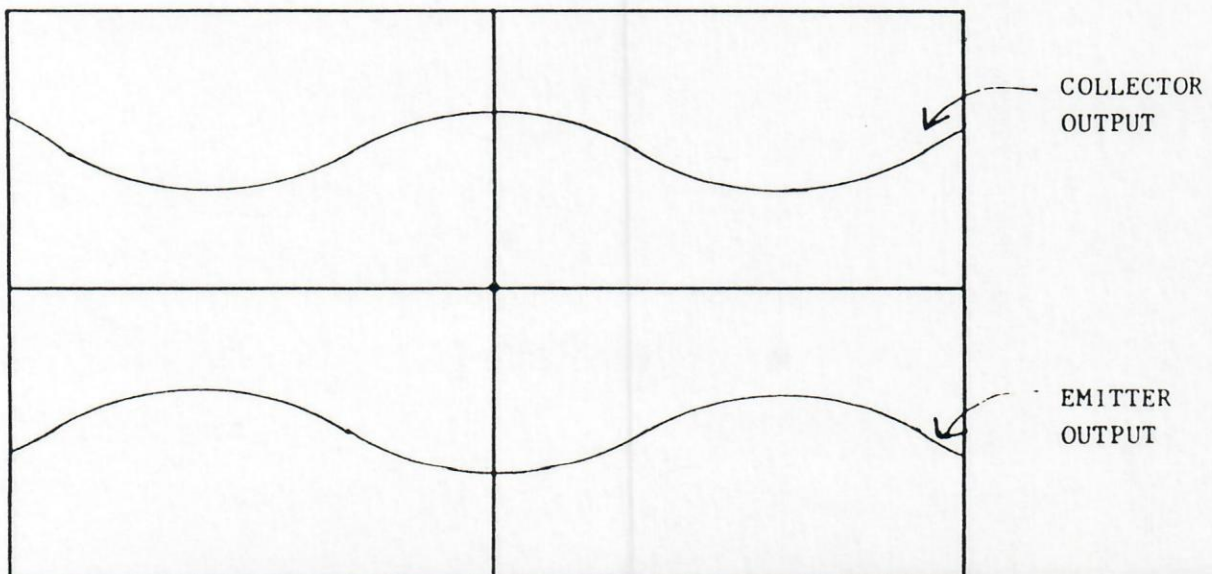


$$V_{in} = 0.2 \text{ volts p-p}$$

$$V_{out} = 4 \text{ volts p-p}$$

$$\text{GAIN} = \frac{V_{out}}{V_{in}} = \frac{4}{0.25} = 16$$

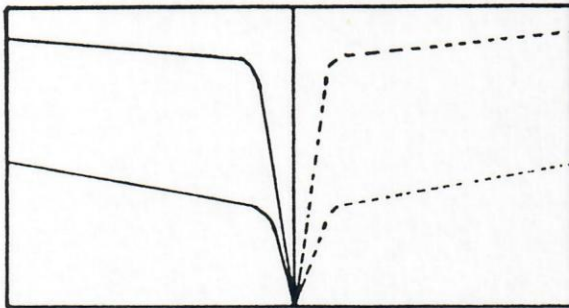
8.



TRANSISTOR CURVE TRACER

This experiment generates the Collector Voltage versus Collector Current Curve for a transistor at two different base currents. Collector Current is sensed as the voltage across the 1K collector resistor. Two Base Currents are generated by the V1 voltage source and the Square Wave Generator. The 0.001ufd capacitor prevents oscillation.

2. Plot of Transistor Characteristic:



Note: The Collector Voltage scale (horizontal) is reversed because the horizontal input is connected to the circuit common with the transistor collector used as reference (common to an oscilloscope)

COMMON BASE AMPLIFIER

A Common Base Transistor Amplifier is tested. The D.C. voltage into the emitter is varied and the input and output voltage is recorded for various input voltages. The input voltage versus output voltage is plotted on a graph and the Amplifier Gain is calculated from the experimental data. The correct bias point for linear operation is also determined. The 1K POT is connected between the +V1 and -V1 supplies so that voltage ranging from +8 volts to -8 volts can be applied to the emitter of the transistor. When the emitter voltage is negative emitter current will flow. The flow of emitter current will cause collector current to flow and the output voltage will change.

The gain of this circuit is given by:

$$I_E = \text{Emitter Current} = \frac{V_{in}}{R_E}$$

$$I_c = I_E = \text{Collector Current}$$

$$V_{out} = V1 - R_c I_c = V1 - \frac{V_{in} R_c}{R_E}$$

neglecting the D.C. Component of the Output voltage

$$V_{out} = \frac{V_{in} R_c}{R_E}$$

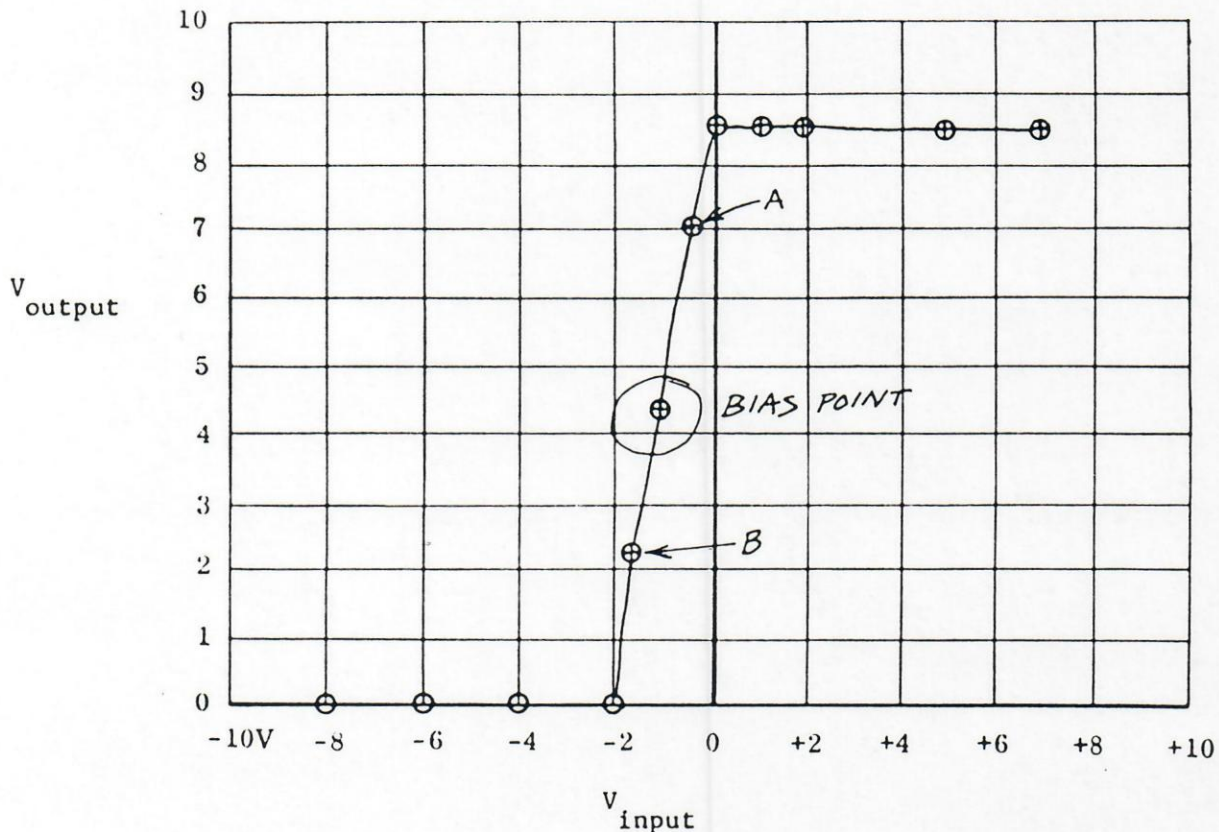
$\text{GAIN} = \frac{V_{out}}{V_{in}} = G = \frac{R_c}{R_E} = \frac{4.7K}{1K} = 4.7$
--

2. Data of Input Voltage and Output Voltage

V _{input}	V _{output}
+7	8.6
+5	8.6
+2	8.6
+1	8.6
0	8.6
-.5	7.0
-1.0	4.4
-1.5	2.2
-2	0
-4	0
-6	0

COMMON BASE AMPLIFIER

3. Graph of V_{input} versus V_{output} from step 2.



4. Calculation of Voltage Gain

$$\text{GAIN} = \frac{\text{change in } V_{\text{out}}}{\text{change in } V_{\text{in}}} = \frac{V_{\text{out}} \text{ at point A} - V_{\text{out}} \text{ at point B}}{V_{\text{in}} \text{ at point A} - V_{\text{in}} \text{ at point B}} = \frac{7.0 - 2.2}{(-0.5) - (-1.5)} = \frac{4.8}{1.0} = 4.8$$

Gain = 4.8

5. The gain is positive for the common base amplifier.
6. The gain in the common emitter amplifier with emitter degeneration in experiment #9 is the same as the gain in this experiment. Since the emitter resistors and the collector resistors are the same in both circuits the gains of the two circuits will be the same.
7. At what input and output voltage would you select the mid operating bias point? Draw this point on the graph. Is the input bias positive or negative?

The proper bias point for linear operation is in the middle of the output voltage variation. Using the curve obtained in paragraph 3 we see that this occurs at $V_{\text{out}} = 4.3$ volts. The input voltage for this point is -1.0 volts.

COMMON BASE A.C. AMPLIFIER

The Common Base A.C. Amplifier is used as a Voltage Amplifier. The Amplifier Voltage Gain is given by the Ratio of the Collector Resistor to the circuit Emitter Resistance. Since the input signal is connected to the transistor emitter, and the output is connected to the collector the current gain is equal to the Alpha of the transistor, or nearly unity.

3. Measurement of A.C. Input and Output Voltages

A. C. V_{out}	=	0.6 volts p-p
A. C. V_{in} at point A	=	2 volts p-p

4. Amplifier Gain

$$GAIN = \frac{A.C. V_{out}}{A.C. V_{in} \text{ at point A}} \times 100 = \frac{0.6}{2} \times 100 = 30$$

GAIN = 30

5. How does this Common Base A.C. Gain compare with the Common Emitter A.C. Gain from Experiment No. 5?

The common emitter has a gain of 111. The common base amplifier has a gain of 30. The voltage gain achieved with the common emitter amplifier is higher than the common base amplifier.

CASCADED AMPLIFIER

Two common emitter amplifiers are connected in series so the gain of the first is followed by the gain of the second amplifier. The input and output voltage magnitudes are measured and the system Gain is calculated. The gain of the first amplifier stage is measured and the theoretical gain of the cascaded amplifiers is calculated. The signal source is the sine-wave output of the signal generator on the Ed-Lab 650. The 100K POT allows the signal level to be adjusted. V_A is the signal voltage on the 1000 to 1 voltage divider consisting of the 110K and 100 ohm series resistors. Therefore, $V_A/1000$ is the actual voltage input into the base of Q4, the first amplifier stage. The output of Q4 is coupled to the base of Q5, the second amplifier stage. The collector output of Q5 is the output voltage from the cascaded amplifiers.

2. The waveform seen at the output should be an understated sine wave. If the signal is distorted the voltage V_A must be reduced by adjusting the 100K POT.
3. A.C. output and V_A voltage

A.C. V_{out} = 3 volts peak to peak

A.C. V_A = 1.0 volts peak to peak

4. Voltage Gain Calculation

The overall gain of the cascaded amplifier stages is the output voltage divided by the input voltage. The output voltage is measured directly at the collector Q5. The input voltage is derived from the voltage at V_A . The actual input voltage is 1/1000 of the voltage measured at V_A .

$\text{TWO STAGE GAIN} = \frac{(\text{A.C. } V_{out})}{(\text{A.C. } V_A)} \times 1000 = \frac{3.0}{1.0} \times 1000 = 3000$
--

5. The single stage gain is measured by measuring the A.C. voltage at the collector of Q4, the first stage amplifier. This voltage is measured at the point marked B.

$\text{ONE STAGE GAIN (G)} = \frac{V_B}{V_A} \times 1000 = \frac{0.05}{1.0} \times 1000 = 50$

Since the output of the first stage is then amplified by the second stage, the total 2 stage gain is the gain of the first stage multiplied by the gain of the second stage.

CASCADED AMPLIFIER

$$\text{THEORETICAL TWO STAGE} = G \cdot G = 50 \times 50 = 2500$$

The actual gain is 3000 and the theoretical gain is 2500.

$$\% \text{ Error} = \frac{3000 - 2500}{3000} \times 100 = \frac{500}{3000} \times 100 = \frac{5}{30} \times 100 = 16\%$$

6. Calculation of the actual input voltage.

$$\text{A.C. } V_{in} = \frac{\text{A.C. } V_A}{1000} = \frac{1.0}{1000} = 1 \text{ millivolt}$$

$$\text{A.C. } V_{in} = 1 \text{ millivolt peak to peak}$$

PNP TRANSISTOR

A common emitter amplifier using a PNP transistor is built. The application of PNP transistors is studied, including the correct polarity of the collector and base voltages for proper operation. The transistor is operated as a D.C. static amplifier and the input voltage versus output voltage is plotted in a graph. The Voltage Gain for this amplifier is measured and the Beta of the transistor is calculated from experimental data.

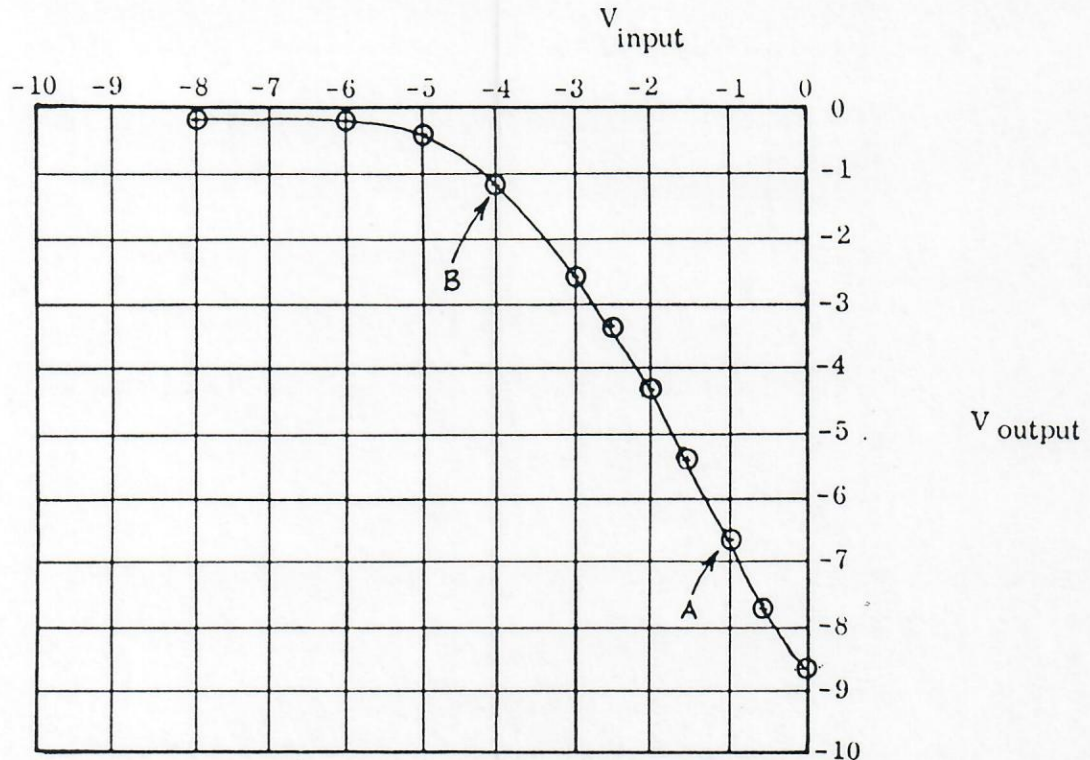
The 1K pot is connected between -V_I and ground so the wiper output can be adjusted from -V_I to ground. This adjustable voltage is applied to the base of Q₁ through the 56K resistor to provide base current. When the base voltage is varied this causes a change in base current. The variation in base current causes a variation in collector current given by $I_C = \beta I_B$. Therefore the current in the 1K collector resistor causes a change in the output voltage. Notice that for proper operation the voltage applied to the PNP Transistor base must be negative with respect to the emitter. The collector voltage must also be negative with respect to the emitter.

2. Data table for Input Voltage and Output Voltage. Note that the meter is connected to measure these negative voltages on the normal meter scale. The minus signs are understood.

V _{input}	V _{output}
-0	- 8.6
-0.5	- 7.8
-1	- 6.6
-1.5	- 5.4
-2.0	- 4.3
-2.5	- 3.3
-3.0	- 2.5
-4.0	- 1.1
-5.0	- 0.3
-6.0	- 0.2
-8.0	- 0.2

PNP TRANSISTOR

3. Graph of the data from the table in step 2.



4. Calculation of Amplifier Voltage Gain. Amplifier voltage gain is calculated from the curve plotted in step 3. Two points on the linear portion of the curve are selected, preferably as far apart as possible. The input and output voltage at these two points are used in the calculation of voltage gain.

$$\text{Voltage Gain} = \frac{V_{\text{out at point B}} - V_{\text{out at point A}}}{V_{\text{in at point B}} - V_{\text{in at point A}}} =$$

$$\frac{(-1.1) - (-6.6)}{(-4.0) - (-1.0)} = \frac{-1.1 + 6.6}{-4.0 + 1.0} = \frac{5.5}{-3.0} = -1.83$$

The voltage gain is negative, that is when the input voltage becomes more negative the output voltage becomes less negative.

5. Calculation of transistor Beta.

$$I_B = \text{Base Current} = \frac{V_{in}}{R_B}$$

$$I_C = \beta I_B = \beta \frac{V_{in}}{R_B}$$

PNP TRANSISTOR

$$V_{out} = I_c R_c = \frac{R_c \beta V_{in}}{R_B}$$

$$\frac{V_{out}}{V_{in}} = \frac{\beta R_c}{R_B} = \text{Gain} = G$$

$$\beta = G \frac{R_B}{R_c} = G \frac{56K}{1K} = G(56)$$

$$\beta = (1.83)(56) \approx 102.5$$

NPN - PNP CASCADED AMP

The Cascaded NPN-PNP Amplifier has the unique feature that the first stage provides both signal and bias to the second stage. This results in a Direct Coupled Cascaded Amplifier, which uses no interstage coupling capacitors. The Direct Coupled feature improves the frequency response of the circuit and allows it to be used at low frequencies and D.C.

2. Data (Output Voltage and Input Voltage)

$V_{out} = 1.5 \text{ volts p-p}$	Peak-to-Peak A.C.
$V_{(point A)} = 0.05 \text{ volts p-p}$	Peak-to-Peak A.C.

3. GAIN Calculation

$$GAIN = \frac{V_{out}}{V_{IN}(pt A)} \times 11 = \frac{1.5}{0.05} \times 11 = 330$$

Gain = 330

4. How does the GAIN compare with the gain for a single stage amplifier/

In Experiment #5 of Unit 6 a high gain Common Emitter A.C. Amplifier was built and the Amplifier Gain was measured as 111. The present circuit under test has a voltage gain three times as large. This is a great improvement.

NOTE: The gain for this type of amplifier is not as high as the gain for the cascaded amplifier. The reason for this is that the first stage transistor, Q4, is operating at a very low collector current quiescent or bias point. The low collector current results in a very high base-emitter resistance, r_{be} which limits the gain of the first stage. For the purposes of calculating it may be noted that the base-emitter resistance is given by the following formula:

$$r_{be} = \frac{25}{I_{collector} \text{ (in milliamps)}} \quad \text{ohms}$$

CONSTANT CURRENT SOURCE

In this experiment we capitalize on the fact that the collector current in a transistor is a function of the base current and is independent of the collector resistance to make a constant current source. The technique is simply to connect a fixed D.C. bias network to the base and emitter to provide constant base current and to use the collector as a constant current source.

2. Emitter Voltage Measurement - Note: For very accurate results use an FET or Digital meter to make your measurements.

$$V_E = 4.25 \text{ volts}$$

3. Calculation of Constant Current

$$I_C = \frac{V_E}{22K} = \frac{4.25}{22K} = 193 \mu a$$

$$I_C = 193 \mu a$$

4. Various Load Resistors are placed in the collector circuit and the collector circuit and the collector current is calculated.

CALCULATE

R_L	READ V_L	$I_L = \frac{V_L}{R_L}$
4.7K	0.9 v	191 μa
15K	2.9 v	193 μa
33K	6.28 v	190 μa
56K	10.44 v	186 μa
100K	14.25 v	142.5 μa
470K	15 v	31 μa
1M	15 v	15 μa
10K	1.94 v	194 μa
3.3K	0.62 v	187 μa
2.2K	0.41 v	186 μa
1K	0.18 v	180 μa
100	0.02 v	200 μa
0 Short	0	no voltage measured no load resistor.

NOTE: Ed-Lab meter of 200K actually loads circuit so that this current calculation is not accurate.

CONSTANT CURRENT SOURCE

5. Is the Load Current constant?

The load current is steady for all loads to within $\pm 10\%$ except in the case of the 100K, 470K, 1 Meg and Open Circuit conditions. With these very high values of load resistance the VI drop across the load resistor exceeds the power supply voltage and the constant current source fails.

EXAMPLE

For the 1 Meg load if 190 μ amps were to flow in the load circuit

$$I \times R = (190 \mu \text{ a}) \times (1 \text{ Meg}) = 190 \text{ volts}$$

The + V1 power supply would have to be 190 volts or more to supply 190 μ amps to a 1 Meg load.

6. Why is the load current reduced for high resistance values?

The power supply does not have enough voltage to provide the required current.

DIFFERENCE CIRCUIT

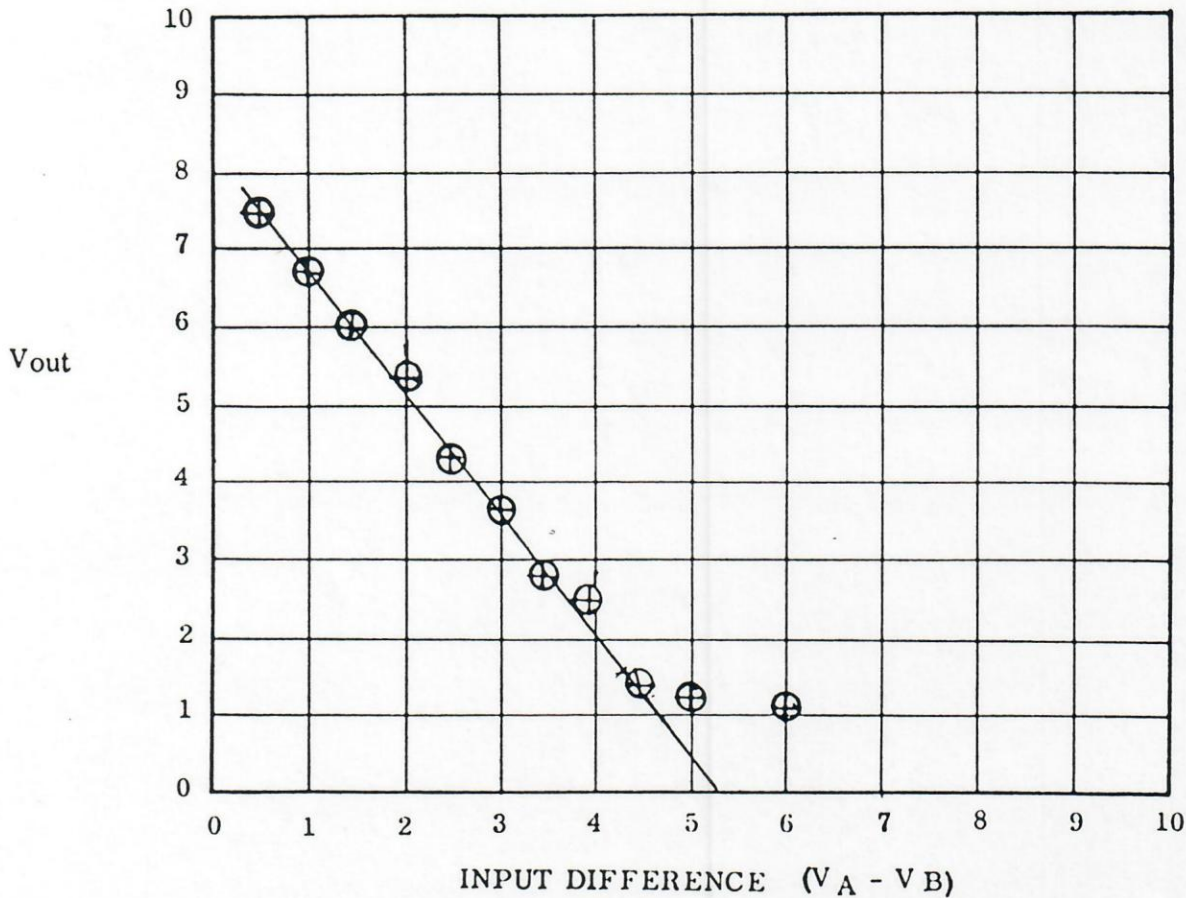
A single transistor amplifier is used as a difference circuit. One signal drives the Base Circuit and the other is connected to the Emitter Circuit. The Base Current is then determined by the Base Resistor and the Voltage difference between the Base and Emitter sources. The operation of this circuit is studied and this experiment serves as an excellent introduction to more sophisticated difference amplifier circuits studied in the following experiments. Note that the Base voltage must be larger than the Emitter voltage in order for this circuit to operate properly. The reverse situation will simply turn the transistor OFF.

2. Data Table V_{in} , V_{out} and $V_{DIFFERENCE}$.

SET		READ	CALCULATE
V_A	V_B	V_{out}	$(V_A - V_B)$
1	0	6.6 v	1.0
1	$\frac{1}{2}$	7.4 v	0.5
3.5	2.0	6 v	1.5
6.0	4.0	5.4 v	2.0
6.0	3.0	3.9 v	3.0
6.0	2.0	2.5 v	4.0
5.0	1.5	2.8 v	3.5
5.0	0.5	1.3 v	4.5
2.0	1.0	6.9 v	1.0
7.0	1.0	1.1 v	6.0
3.5	1.0	4.2 v	2.5
6.0	1.0	1.1 v	5.0

DIFFERENCE CIRCUIT

3. Graph of recorded results.



4. Does the output correspond to the difference between inputs?

The graph of step 3 shows that there is a considerable linear portion of the circuit response where the V_{out} is proportional to the Difference Voltage.

5. Calculation of Difference Gain

$$\text{DIFFERENCE GAIN} = \text{slope} = \frac{\Delta V_{out}}{\Delta (V_A - V_B)} = \frac{-8.2}{5.4} = -1.5$$

DIFFERENCE GAIN = - 1.5

6. Is the Difference Gain positive or negative?

The Difference Gain is Negative because an increase in Difference Voltage causes a decrease in the Output Voltage.

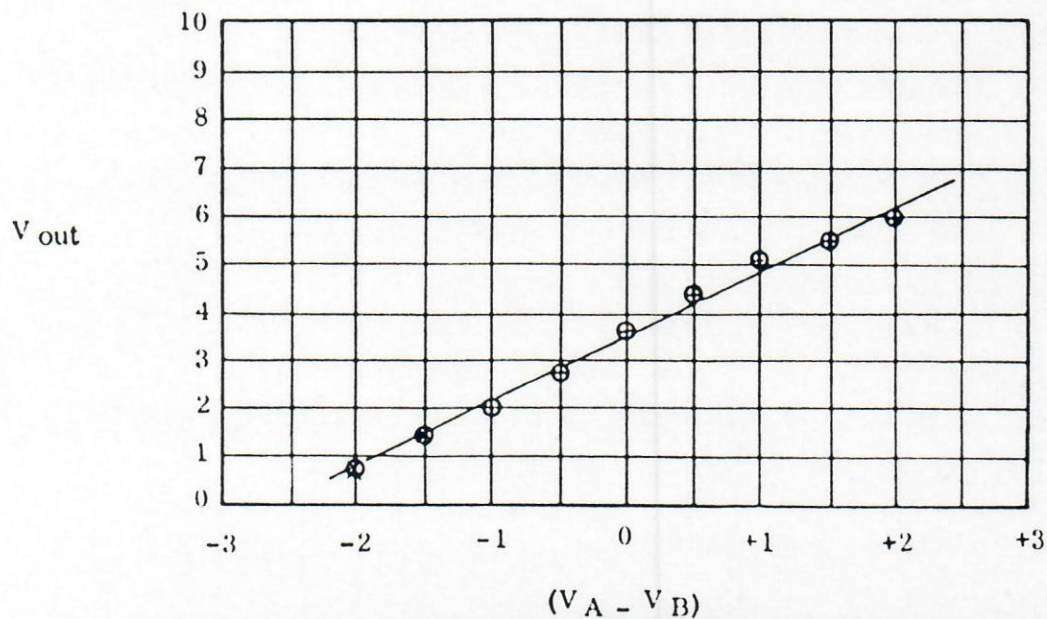
DIFFERENCE AMPLIFIER

A two transistor Difference Amplifier is built and tested. This difference circuit shows the typical symmetry encountered when examining the circuit diagrams for commercial operational amplifiers.

2. Data Table

V_A	V_B	V_{out}	$(V_A - V_B)$
0	0	3.8 v	0
0	.5	2.8 v	-0.5
0	1	2.0 v	-1.0
0	1.5	1.5 v	-1.5
0	2	0.8 v	-2.0
.5	0	4.4 v	+ .5
1.0	0	5.0 v	+1.0
1.5	0	5.5 v	+1.5
2	0	6.0 v	+2
.5	1	2.8 v	-.5

3. Graph of results.



DIFFERENCE AMPLIFIER

4. Calculation of Difference Gain

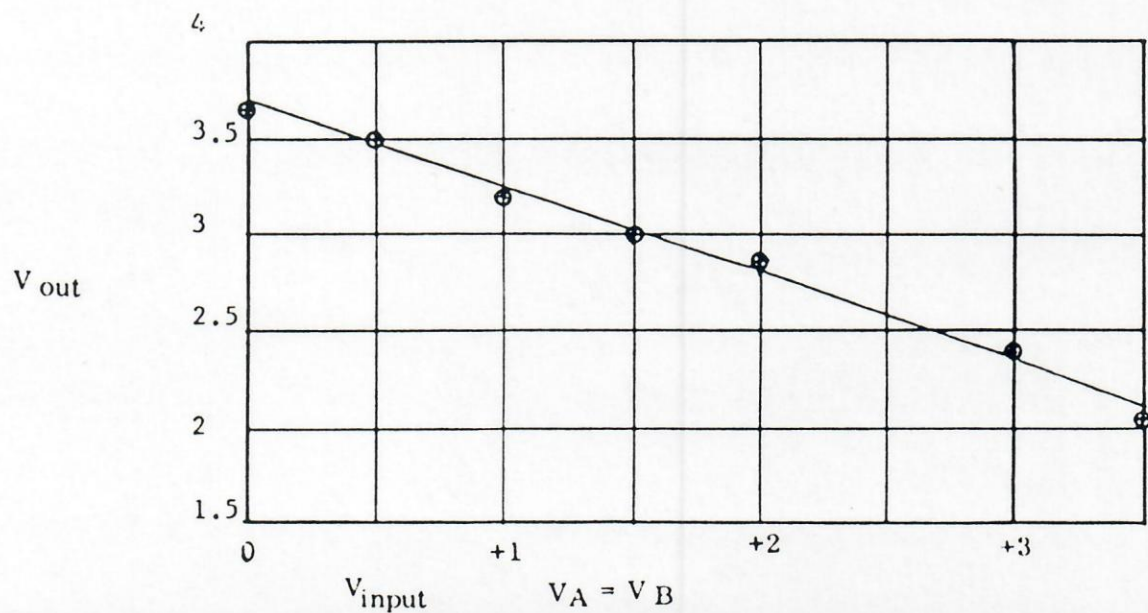
$$\text{DIFFERENCE GAIN} = \frac{\Delta V_{\text{out}}}{\Delta (V_A - V_B)} = \frac{5.2}{4.0} = 1.3$$

DIFFERENCE GAIN = 1.3

5. Common Mode Gain Data

$V_A = V_B$	V_{out}
0	3.7
0.5	3.5
1.0	3.2
1.5	3.0
2.0	2.8
2.5	2.6
3.0	2.4
4.0	2.1

6. Graph of Common Mode Gain Data



DIFFERENCE AMPLIFIER

7. Calculation of Common Mode Gain

$$\text{COMMON MODE GAIN} = \frac{\Delta V_{\text{out}}}{\Delta V_A} = \frac{1.6}{4.0} = 0.4$$

$$\text{Common Mode GAIN} = 0.4$$

8. Common Mode Rejection Ratio

$$\text{CMRR} = \frac{\text{Difference Gain}}{\text{Common Mode Gain}} = \frac{1.3}{0.4} = 3.25$$

$$\text{CMRR} = 3.25$$

Note that the Common Mode Rejection Ratio for this difference amplifier is much lower than the typical values for CMRR found in commercial operation amplifiers. This is primarily because the difference gain is low (1.3)

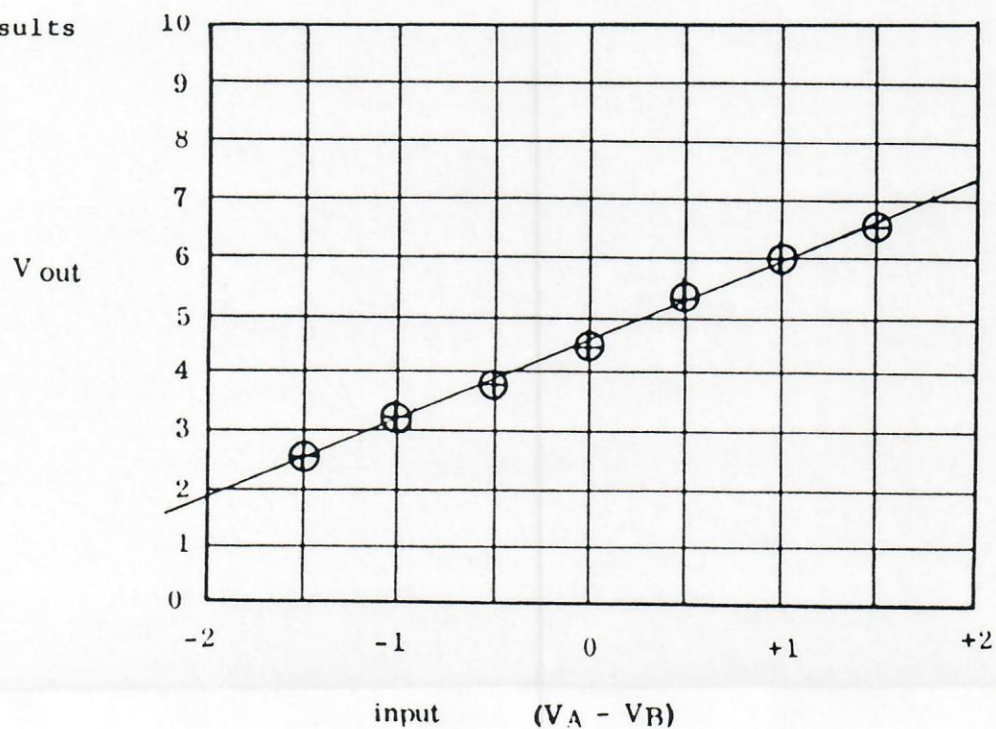
CONSTANT CURRENT DIFFERENCE AMPLIFIER

This experiment is an expansion of Experiment No. 20 (DIFFERENCE AMPLIFIER) in that the emitter of the difference amplifier is now supplied by a constant current source as studied in Experiment No. 18, (CONSTANT CURRENT SOURCE). This will result in an improvement in the Common Mode Rejection Ratio.

2. Data Table

V_A	V_B	V_{out}	$(V_A - V_B)$
0	0	4.6	0
0	0.5	3.8	-0.5
0	1	3.1	-1
0	1.5	2.6	-1.5
.5	0	5.3	+0.5
1	0	6.0	+1
1.5	0	6.6	+1.5
.5	.5	4.6	0
.5	1.0	3.9	-0.5
1	.5	5.3	+0.5
1	1	4.5	0

3. Graph of Results



CONSTANT CURRENT DIFFERENCE AMPLIFIER

4. Calculation of Difference Gain

$$\text{DIFFERENCE GAIN} = \frac{\Delta V_{out}}{\Delta V_A - V_B} = \frac{7.4 - 1.8}{4} = \frac{5.6}{4} = 1.4$$

DIFFERENCE GAIN = 1.4

5. Data Table Common Mode Gain

$V_A = V_B$	V_{out}
0	4.6
1	4.6
2	4.6
3	4.6

Note: The V_{out} will be very steady. A very accurate Digital Voltmeter must be used, or a potentiometric voltmeter as described in UNIT 1 Experiment No. 14.

6. Calculation of Common Mode Gain

$$\text{Common Mode Gain} = \frac{\Delta V_{out}}{\Delta V_A} = \frac{0.005}{4} = 0.001$$

Common Mode Gain = 1×10^{-3}

7. Calculation of Common Mode Rejection Ratio

$$\text{CMRR} = \frac{\text{DIFFERENCE GAIN}}{\text{COMMON MODE GAIN}} = \frac{1.4}{1 \times 10^{-3}}$$

CMRR = $1.4 \times 10^3 = 1400$

How does the CMRR with the Constant Current Source compare with the CMRR with the emitter resistor from the previous experiment?

This is a much improved CMRR, about 500 times better. The improvement is a result of the Emitter current being constant, holding the amplifier collector currents constant in the Common Input mode.

DARLINGTON AMPLIFIER

Two NPN Transistor Emitter follower amplifiers are connected in series to form a Darlington Amplifier. This allows the low impedance 4 ohm speaker to be driven from the Signal Generator in series with a 33K input resistor.

The signal generator triangle output is connected to the 10K pot to allow the input signal level to be adjusted. This input signal drives the base of Q4. The emitter of Q4 drives the base of Q5. Therefore, the current gain of the two transistors is the product of the Beta of the two transistors. This type of Darlington Amplifier has a very large current Gain. The input impedance is very high for this circuit, even though the load is a 4 ohm speaker. The input impedance is the load resistance times the beta of transistor 1 times the beta of transistor 2.

$$R_{in} = R_{LOAD} \cdot \beta_1 \cdot \beta_2$$

2. The level of the input signal must be adjusted so that the transistors are operating in the linear range. The input 10K POT should be adjusted for the maximum input signal that will provide an undistorted output signal as observed on the oscilloscope.

AUDIO DRIVER

A COMPLEMENTARY OUTPUT EMITTER FOLLOWER Audio Driver is built. The Audio Driver is tested for various input frequencies. The Voltage Gain is calculated from the measurement of the input and output voltages. The input power and output power are calculated from the experimental data and the amplifier power gain is found.

The signal generator triangle output is used to drive the 10K input signal level adjusting POT. This input signal then drives the base of the emitter follower Q5. The load on Q5 is the 1K resistor in parallel with the input circuit to the two complementary emitter follower transistors Q4 and Q3. Note that the 1K load on Q5 is connected to -V2 so the emitter of Q5 can be positive or negative depending on the input voltage. When the emitter of Q5 is positive, transistor Q4 will be turned ON and current from the emitter of Q4 will drive the speaker. When the emitter of Q5 is negative then Q3 will be turned ON and the emitter of Q3 will drive the speaker. Therefore, there are actually two emitter follower amplifiers connected to the speaker, an NPN emitter follower for the positive signals and a PNP emitter follower for the negative signals. The NPN and PNP emitter followers are called COMPLEMENTARY EMITTER FOLLOWERS.

4. Measurement of Audio Drive Voltage Gain

$$\text{A.C. } V_{in} = 2.4 \text{ volts peak to peak}$$

$$\text{A.C. } V_{out} = 2.4 \text{ volts peak to peak}$$

$$\text{Voltage Gain} = \frac{\text{Output Voltage}}{\text{Input Voltage}} = \frac{\text{A.C. } V_{out}}{\text{A.C. } V_{in}} = \frac{2.4}{2.4} = 1$$

$$\text{Voltage Gain} = 1$$

5. Output Power Calculation

In order to calculate the output power delivered to the speaker we must calculate the RMS output voltage across the speaker.

$$V_{out \text{ RMS}} = \frac{1}{2} (0.707) (V_{out \text{ peak to peak}})$$

$$V_{out \text{ RMS}} = 0.85 \text{ volts RMS}$$

The Output Power is:

$$\text{Output Power} = \frac{(V_{out \text{ RMS}})^2}{R_L} = \frac{(V_{out \text{ RMS}})^2}{4} = \frac{(0.85)^2}{4} = 0.18 \text{ watts}$$

$$\text{Output Power} = 0.18 \text{ watts}$$

AUDIO DRIVER

6. Input Power Calculation

The calculation of input power is performed by first measuring the peak to peak voltage across the 10K input resistor, A.C. V_B . This voltage is connected to the $V_{B\text{RMS}}$, the RMS voltage across the 10K resistor.

A.C. V_B peak to peak = 0.6 volts peak to peak

$$V_{B\text{RMS}} = \frac{1}{2}(0.707)(\text{A.C. } V_B \text{ peak to peak}) = \frac{1}{2}(0.707)(0.6) = 0.212 \text{ volts RMS}$$

Using Ohms Law the RMS current into the Audio Driver input can be calculated:

$$I_{\text{in RMS}} = \frac{V_{B\text{RMS}}}{10\text{K}} = \frac{0.212}{10\text{K}} = 2.12 \times 10^{-5} \text{ amps}$$

The peak to peak input voltage between the base of Q5 and ground is measured using the oscilloscope. This can be connected to RMS voltage by applying the formula.

$$V_{\text{in peak to peak}} = 0.4 \text{ volts peak to peak}$$

$$V_{\text{in RMS}} = \frac{1}{2}(0.707)(\text{A.C. } V_{\text{in}}) = \frac{1}{2}(0.707)(2.4) = 0.85 \text{ volts RMS}$$

$$V_{\text{in RMS}} = 0.85 \text{ volts RMS}$$

$$\text{INPUT POWER} = (V_{\text{in RMS}})(I_{\text{in RMS}}) = (2.12 \times 10^{-5})(0.85) = 1.8 \times 10^{-5} \text{ watt}$$

$$\text{INPUT POWER} = 1.8 \times 10^{-5} \text{ watts} = 18 \text{ microwatts}$$

AUDIO DRIVER

7. Calculation of Power Gain

Power Gain is the increase in power caused by the amplifier.

$$\text{Power Gain} = \frac{\text{Output Power}}{\text{Input Power}} = \frac{0.18}{1.8 \times 10^{-5}} = 10^4 = 10,000$$

Power Gain = 10,000

FEEDBACK AMPLIFIER

Feedback is utilized to stabilize the gain of the amplifier. The student will connect this circuit and test it for various levels of feedback. Since the feedback is negative, the larger the amount of feedback, the lower the overall gain of the amplifier will be. The important point is that the gain remains stable for variations in the individual transistor Beta's. At high amplifier gain the student will place the microphone near the speaker and cause the system to oscillate. The amplifier gain will then be lowered to stop the oscillation.

The microphone output drives the base of collector biased transistor amplifier Q6. This stage is a common emitter microphone amplifier. The collector of Q6 is the input to the actual feedback amplifier. This point is labeled "input E". The microphone amplifier Q6 is A.C. coupled to the base of Q5. The output of common emitter amplifier Q5 drives the bases of the two complimentary output transistors Q4 and Q3. The Diode D4 keeps the base of Q4 one diode drop above the base of Q3 and assures that both output transistors will never be on at the same time. When the Q5 collector signal is high transistor Q4 is on and current flows into the A.C. coupled speaker S. The 100ufd coupling capacitor will charge up to the average voltage of the output signal. When the collector of Q5 decreased below the average voltage of the signal, Q4 will turn off and Q3 will turn on. The negative half of the signal will drive the output through Q3. The output voltage is connected to the 100K feedback pot connected to the base of Q5. When the output voltage increases, the feedback pot will cause the base of Q5 to increase and counteract the increasing output. Thus the feedback is negative and reduces and stabilizes the overall gain of the amplifier.

4. Measurement of the output waveform with an audio input into the microphone.

$$V_{\text{output (peak-to-peak)}} = 2 \text{ v p-p}$$

6. Record of $V_{\text{oscillation}}$

$$V_{\text{oscillation(peak to peak)}} = 3 \text{ v p-p}$$

- 8.

$$V_{\text{output (point X) (peak-to-peak)}} = 1.5 \text{ v p-p}$$

- 10.

$$R_f = 10K$$

- 11.

$$V_{\text{in (point E) peak-to-peak}} = 0.05 \text{ v p-p}$$

FEEDBACK AMPLIFIER

12. Amplifier Gain:

$$\text{Gain} = \frac{V_{\text{output}} \text{ (Point X) peak to peak (no oscillation)}}{V_{\text{in}} \text{ (Point E) peak to peak}} = \frac{1.5}{0.05} = 30$$

$$\text{GAIN} = 30$$

13.

$$\text{MAX GAIN} = \frac{2}{0.05} = 40$$

FET OPERATION

The student will connect the FET in a D.C. TEST CIRCUIT and measure the V/I characteristics of the DRAIN terminal verses the GATE voltage.

Note: The FET is protected against burnout. The Gate Junction may be forward biased without damage to the FET.

2.

V_{in} SWITCH A DOWN	V_{out} SWITCH A UP
-8	+9.39
-6	+9.40
-4	+9.39
-2	+7.63
-1.8	+6.33
-1.6	+5.04
-1.4	+3.48
-1.2	+2.16
-1.0	+1.29
-0.8	+0.95
-0.6	+0.76
-0.4	+0.65
-0.2	+0.58
0.0	+0.51
+0.5	+0.40
+1.0	+0.33
+2.0	+0.24
+4.0	+0.15
+6.0	+0.11
+8.0	+0.09

FET OPERATION

3.

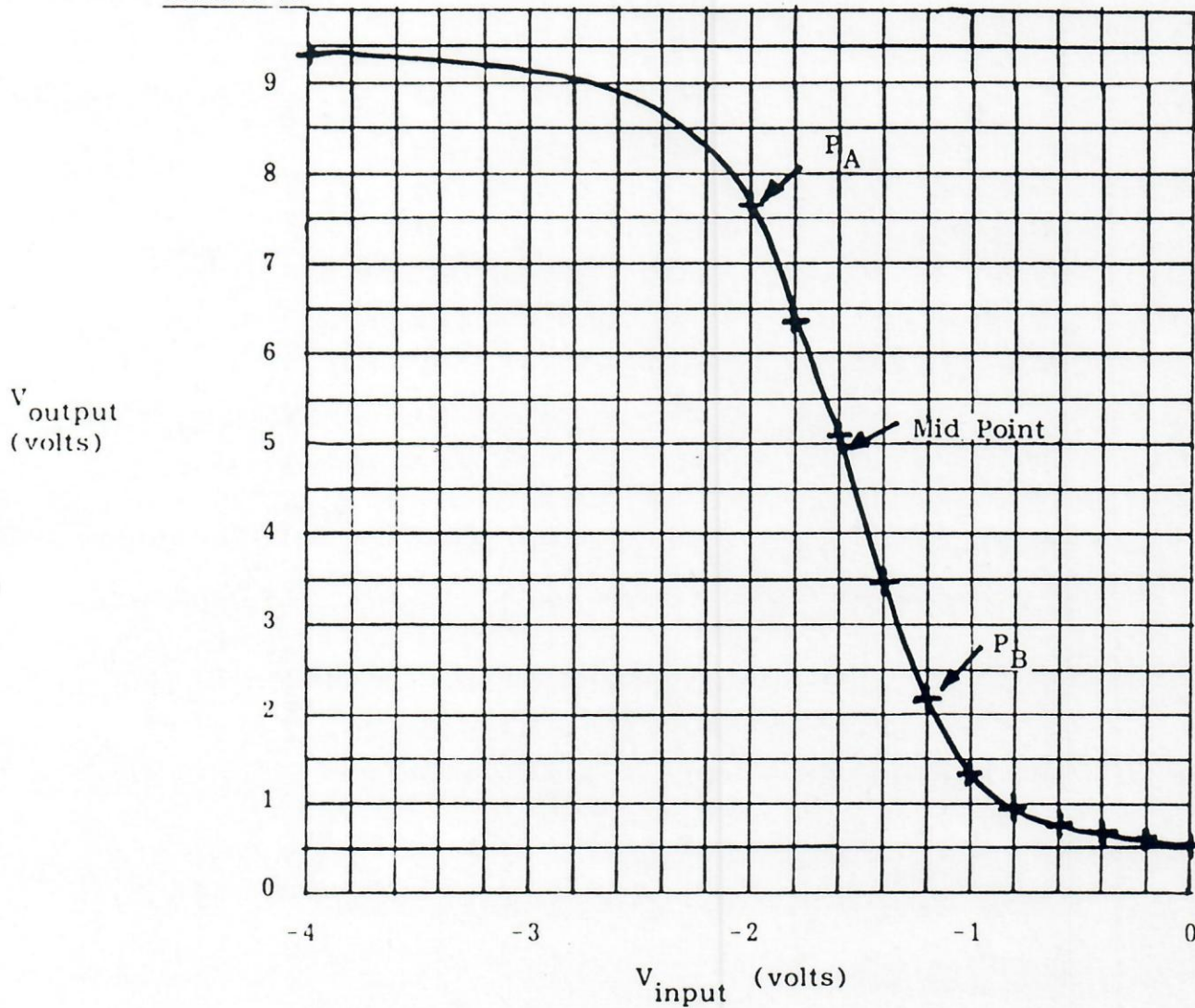
GRAPH #1

V_{output}
(volts)



FET OPERATION

GRAPH #2



4. Graph #2 of step 3 has a linear region where the curve has a straight slope. Label a point of the curve at the top of the linear region (P_A). Label a point at the bottom of the linear region (P_B).

For P_A :

$V_{\text{out}} = \underline{\quad 7.63 \quad}$

$V_{\text{in}} = \underline{\quad -2 \quad}$

FET OPERATION

FOR P_B :

$$V_{out} = \underline{2.16}$$

$$V_{in} = \underline{-1.2}$$

5. Calculate the mid-point of the linear region.

$$V_{out} \text{ (mid point)} = \frac{V_{out A} - V_{out B}}{2} + V_{out B} =$$

$$\frac{(7.63) - (2.16)}{2} + (2.16) = \underline{4.90}$$

Label the V_{out} (mid point) on the graph of step 3.

Record the Input V_{in} for the mid point. This mid-point would correspond to the normal input bias voltage.

$$V_{in} \text{ (mid point)} = \underline{-1.50}$$

6. Calculate the D.C. Gain of the FET Amplifier in this circuit.

$$\text{GAIN} = \frac{\Delta V_{out}}{\Delta V_{in}} = \frac{V_{out A} - V_{out B}}{V_{in B} - V_{in A}} = \frac{(7.63 - 2.16)}{(-1.2 - 2)} = 6.84$$

$$\text{GAIN} = 6.84$$

7. Calculate the FET Transconductance.

$$\text{Transconductance} = g_m = \frac{\Delta I_{out}}{\Delta V_{in}} = \frac{\Delta V_{out}}{R_L} = \frac{\text{GAIN}}{R_L}$$

Note that transconductance has the units of $\frac{1}{\text{ohm}}$ or mho

$$g_m = \frac{\text{GAIN (of Step 6)}}{R_L} = \frac{(6.84)}{3.3K} = \underline{\hspace{2cm}} 2.07 \text{ millimho}$$

FET OPERATION

$$g_m = 2070 \text{ MICROMHO}$$

g_m is usually written in terms of MICROMHOS. The answer should be on the order of 1000 micromhos.

QUESTIONS:

1. Since the Gate Junction is reverse biased in the linear region of operation of the FET, would you say the gate impedance is high or low? When a P-N Junction is REVERSE BIASED, the impedance or resistance is very high.
2. Can the current in the FET Drain - Source Circuit be turned nearly OFF with the gate? YES. The DRAIN CURRENT of the FET is very nearly ZERO for large negative GATE VOLTAGES. To see this, note that in GRAPH #1 of step 3 for a GATE VOLTAGE of -8 volts the DRAIN VOLTAGE is 9.38 volts. This DRAIN VOLTAGE is the same as the POWER SUPPLY VOLTAGE indicating that there is no current flow in the FET. Under these conditions we say the FET is OFF.
3. Can the FET be used as a Solid-State Switch? Yes, the FET can be used as a SOLID STATE SWITCH. Large Negative Gate Voltage turn the FET OFF. Gate Voltages near Zero turn the FET ON.
4. Which portions of the graph show that the FET can be used as a Switch? Looking at GRAPH #1 the region to the left of Input Voltage -4 volts indicates the area where the FET is OFF (High Drain Voltage, indicating very low Drain Current). The region of GRAPH #1 to the right of Input Voltage -2 Volts (Towards Positive Input Voltage) is the Region where the FET is ON (Low Drain Voltage indicates that the FET Drain is carrying a large current).
5. What would the gain of this amplifier be if the load resistor was changed to 10K?

$$\text{GAIN} = g_m \times R_L = (2070 \text{ micromho}) \times 10K = 20$$

$$\text{GAIN (for } 10K R_L \text{ Resistor)} = 20$$

FET OPERATION

6. At what V_{GS} voltage would you normally bias the FET Amplifier in this experiment? The FET is normally biased in the middle of the LINEAR REGION. This is the V_{out} (mid point) calculated in step 5. The results in step 5 were to measure a V_{in} (mid point) of -1.50 volts. This would be the normal Input Voltage Bias Point for this FET Amplifier.

FET COMMON SOURCE AMPLIFIER

The student builds and tests a FET Common Source A.C. Amplifier with Source Bias. The 100K pot connected to the FET Source allows adjustment of the D.C. bias point (Source Voltage Positive with respect to the Gate). The $0.25\mu\text{fd}$ capacitor from the FET Source to Ground provides an A.C. bypass of the Source Resistor, connecting the Source to Ground for the A.C. Signal. The Amplifier Output Signal appears at the FET Drain.

4. Record the Input Voltage and Output Voltage Amplitude (peak to peak)

$$V_{\text{input}} = 0.3 \text{ Vp-p}$$

$$V_{\text{output}} = 1.9 \text{ Vp-p}$$

5.
$$\text{GAIN (voltage)} = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{1.9}{(0.3)} = 6.33$$

6.
$$g_m \text{ (from Experiment No. 25)} = 2070 \times 10^{-6}$$

$$\text{GAIN (voltage)} = g_m R_L = (2.07) (3.3\text{K}) =$$

$$\text{GAIN}_v = 6.81$$

7. How does the theoretical gain calculated in step 6 compare to the actual gain measured in step 5? The measured gain and the theoretical gain are within 10% of each other. The agreement is good.
8. Increase the Input Signal Amplitude until the Output Signal just begins to distort. Record the Maximum Output Amplitude.

$$\text{Output Amplitude max.} = 5 \text{ Vp-p}$$

FET COMMON DRAIN AMPLIFIER

The student builds and tests a COMMON DRAIN or SOURCE FOLLOWER FET circuit. This circuit has a GAIN of slightly less than 1 making it unsuitable for a VOLTAGE AMPLIFIER, however, the OUTPUT IMPEDANCE is LOW allowing it to drive low resistance loads at HIGH CURRENT and providing POWER AMPLIFICATION.

- Adjust the Input Voltage Amplitude to a convenient level.
Record the Input Voltage Amplitude and the Output Voltage Amplitude.

$V_{\text{input}} = 1.0 \text{ volts p-p}$
$V_{\text{output}} = 0.9 \text{ volts p-p}$

- Calculate the circuit GAIN.

$$\text{GAIN} = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{(0.9)}{(1.0)} = 0.9$$

$\text{GAIN} = 0.9$

- Place Switch C UP (10K load). Record V_{load} .

$V_{\text{load}} = 0.89 \text{ Vp-p}$

- Calculate the Output Impedance of the circuit.

$$R_{\text{out}} = \frac{(V_{\text{out no load}} - V_{\text{out load}})}{V_{\text{out load}}} R_L$$

$$R_{\text{out}} = \frac{[(0.9) - 0.89] \times 10\text{K}}{(0.89)} = 112 \Omega$$

$R_{\text{out}} = 112 \Omega$

FET COMMON SOURCE AMPLIFIER

QUESTIONS:

1. How does the voltage gain of the FET A.C. Common Source Amplifier from this experiment compare to the gain of a similar Common Emitter Transistor D.C. Amplifier experiment? The gain of the FET Common Source Amplifier and the Common Emitter Amplifier are similar in magnitude and in phase.
2. Is the Gate Junction forward biased or reverse biased in the normal operating range? The Gate Junction is Reverse Biased in the normal operating range of the amplifier. This means that the Gate is Negative with respect to the Source.
3. To what Transistor Amplifier circuit is the FET Common Source Amplifier similar? The FET Common Source Amplifier is similar to the Transistor Common Emitter Amplifier. The difference is that the transistor Amplifier Base is biased Positively with respect to the Emitter.

FET COMMON DRAIN AMPLIFIER

QUESTIONS:

1. If we assume the FET gate draws no current (infinite impedance) what is the input impedance for the circuit in Figure 27-1?
If the Input Circuit draws ZERO CURRENT then the INPUT IMPEDANCE of the circuit in figure 27-1 will be 1 Megohm, the value of the resistor connected from the Gate to Ground.
2. Will the Current Gain of this circuit be high or low? The CURRENT GAIN will be HIGH.
3. Calculate the Current Gain (assuming voltage gain of 1).

$$\text{Current Gain} = \frac{R_{in}}{R_{load}} \quad \text{where } R_{Load} = 10K$$

$$\text{Current Gain} = \frac{R_{in}}{R_{load}} = \frac{1 \text{ Meg}}{10K} = 100$$

4. Is the gain less than 1 as expected?
The Voltage gain calculated in step 4 for this circuit is 0.9.
This value is less than 1 as expected.

FET COMMON GATE AMPLIFIER

The student will build and test a COMMON GATE FET AMPLIFIER. In this circuit the signal is applied to the SOURCE and the output is connected to the DRAIN.

3. Record the Amplitude of the Input and Output Signals.

$$V_{in} = 0.15 \text{ Vp-p}$$

SWITCH A DOWN

$$V_{out} = 1.6 \text{ Vp-p}$$

SWITCH A UP

4. Calculate the Voltage Gain of the circuit.

$$\text{GAIN} = \frac{V_{out}}{V_{in}} = \frac{(1.6)}{(0.15)} = 10.6$$

$$\text{GAIN} = 10.6$$

5. Calculate the Theoretical value of the circuit voltage gain using,

$$\text{GAIN} = g_m R_L$$

g_m = Transconductance (measured in Exp. No. 1)

R_L = Load Resistance = 33K

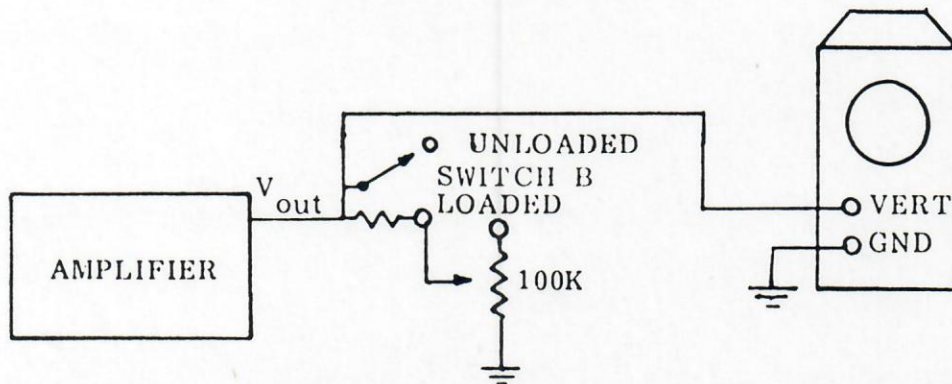
$$\text{GAIN} = (2.07) (33) = 68.3$$

6. The theoretical and measured gain of the circuit are not in very close agreement because of the non-linear nature of the FET Transconductance.

FET COMMON GATE AMPLIFIER

QUESTIONS:

1. Verify the Output Impedance of the circuit. The Output Impedance should equal $R_L = 33K$.
 - a) Sketch the Circuit you will use to measure output impedance.



- b) Describe the procedure

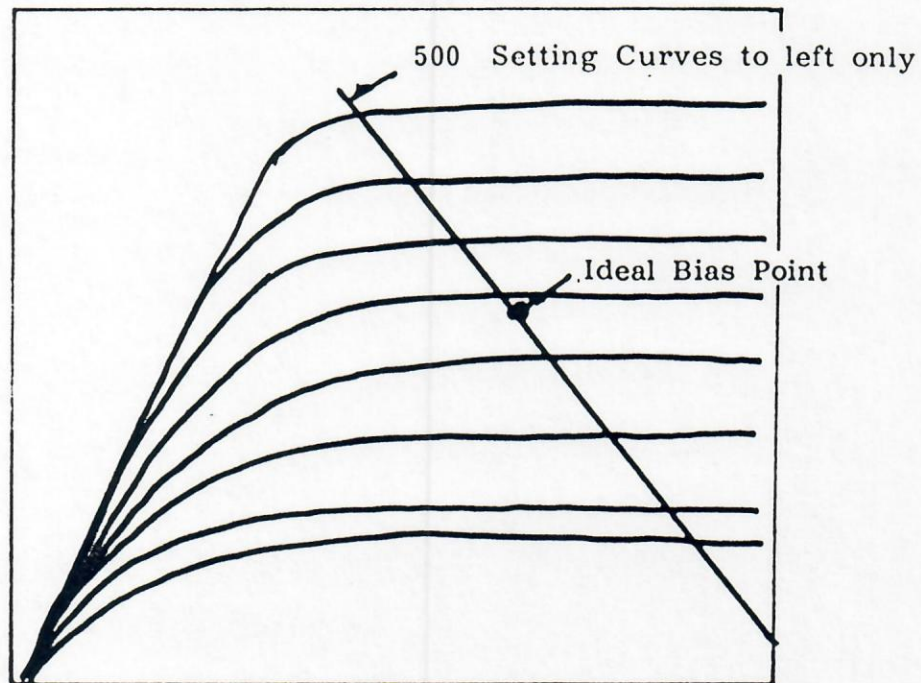
PROCEDURE:

1. Set the Switch to the Unloaded position.
 2. Adjust the Output Voltage to a convenient level.
For example 2 volts peak to peak.
 3. Place the Switch in the Loaded position.
 4. Adjust the 100K load pot until the Loaded Output is half the unloaded output.
 5. Record the setting of the potentiometer.
The resistance of the pot is equal to the output impedance.
- c) If a trainer is available, perform the measurement of output impedance.

FET CHARACTERISTIC

The student generates a "Family" of FET characteristic curves which are displayed on the oscilloscope.

4. Sketch the family of characteristic curves obtained.



QUESTION:

1. What is the ideal bias point (Gate Source Voltage) for a FET linear amplifier as seen on the Characteristic Curve, for a load resistance of 500 ohms?
The ideal bias point for the FET with a load of 500 ohms will be the bias level that results in a Quiescent or D.C. Drain Voltage midway between the maximum and minimum Drain voltages achieved on the family of curves with 500 ohm load. This point is indicated in the graph shown in step 4.

FET CONSTANT CURRENT SOURCE

The student builds and tests a FET SOURCE FOLLOWER circuit with feedback from the Source circuit to the Gate to maintain a constant current in the load resistor R_L .

3. Change R_L to the values indicated in the table below. Record the voltage V_L reading of the meter for each load resistor.

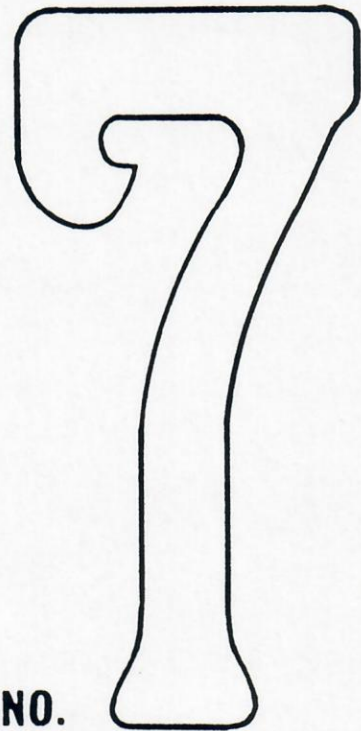
R_L LOAD RESISTOR	V_L METER READING	CALCULATE $I_L = \frac{V_L}{R_L}$ LOAD CURRENT
1K	1V	1ma
100 ohm	0.1V	1ma
2.2K	2.1V	0.95ma
3.3K	3.2V	0.96ma
4.7K	4.7V	1.0ma
10K	9.9V	0.99ma
15K	15V	1.0ma
22K	17V	0.77ma
33K	17V	0.51ma

5. Does the circuit operate as a constant current source?
The circuit is a constant current source with excellent accuracy within the limits of proper operation. The constant current source fails when the voltage required to maintain the constant current in the load resistor exceeds the Power Supply Voltage.
6. For which load resistors does the Constant Current Source fail to generate 1 ma? The constant current source fails for the 22K and 33K load resistors. This is because the Power Supply voltage is not high enough to supply 1 ma to these load resistors.



Ed-Lab
ANSWER MANUAL

VACUUM TUBES



UNIT NO.
CES INDUSTRIES, INC.

TRIODE D.C. AMPLIFIER

The Triode Amplifier is used as a Voltage Amplifier in the Common Cathode configuration. Note that this circuit is being tested for D.C. characteristic. The Input and Output voltages are plotted point by point.

3. Table of Input Versus Output Voltage.

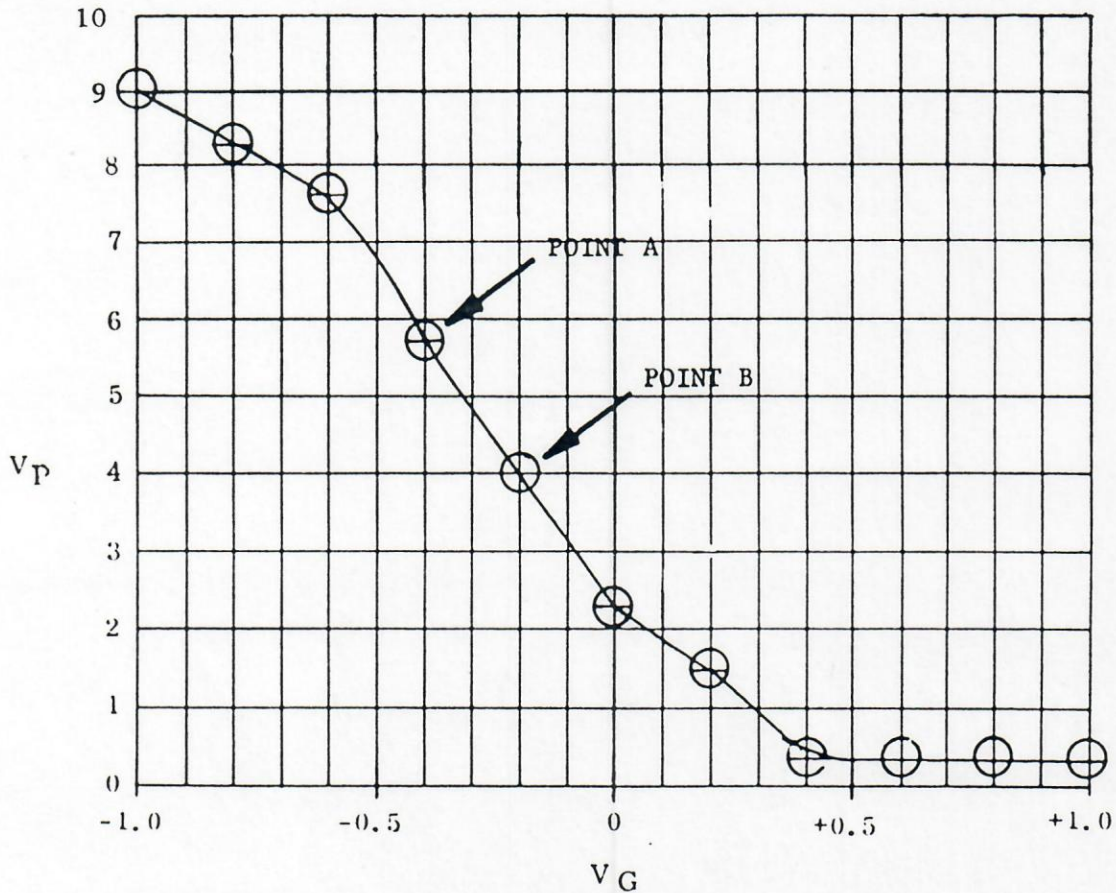
$V_{\text{input}} (V_G)$	$V_{\text{output}} (V_P)$
-7	9.2
-6	9.2
-4	9.2
-2	9.2
-1	9.0
-0.8	8.3
-0.6	7.6
-0.4	5.7
-0.2	4.0
0.0	2.2
+0.2	1.4
+0.4	0.2
+1	0.2
+3	0.2
+6	0.2

Area of V_{input} where
 V_{output} changes rapidly
-1 volt to +0.4 volts.

Note: The student must select data to be taken at small increments of V_G for the portion of the curve where V_P (output voltage) varies with V_G .

TRIODE D.C. AMPLIFIER

4. Graph of the results from step 3.



Selection of the Linear Operating Range

LINEAR RANGE	V_{input}	FROM 0.5 volts to 0.0 volts
	V_{output}	FROM 7.5 volts to 2 volts

MID-BIAS POINT

$V_{plate\ voltage} = 5\ volts$

$V_{grid\ voltage} = -0.3\ volts$

5. Amplifier Gain

	V_{in}	V_{out}
POINT A	-0.4	5.7
POINT B	-0.2	4.0

$$GAIN = \frac{V_{out\ A} - V_{out\ B}}{V_{in\ A} - V_{in\ B}} = \frac{(5.7) - (4.0)}{(-0.4) - (-0.2)} = \frac{-1.7}{0.2} = -8.5$$

AMPLIFIER GAIN = -8.5

TRIODE CHARACTERISTICS

The Plate Resistance r_p and the Amplification Factor μ are determined for the tube used in the common cathode configuration

5. Data Table

SWITCH B UP	measure		calculate	
	adjust V_{cc} SWITCH A UP	SWITCH A DOWN	$V_L = V_{cc} - V_p$	$I_p = \frac{V_L}{22K}$
POINT 1	$V_{cc1} = 8$ volts	(vary V_G for) $V_p = 3$ volts	$V_{L1} = 5$ volts	$I_{p1} = \frac{5}{22K} = 227 \mu a$
POINT 2	$V_{cc2} = 5$ volts	(same V_G) $V_p = 1.54$ v	$V_{L2} = 3.46$ v	$I_{p2} = 157 \mu a$

7. Calculation of Plate Resistance.

$$r_p = \frac{V_p}{I_p} = \frac{(V_{p1} - V_{p2})}{(I_{p1} - I_{p2})} = \frac{3 - 1.54}{(227 - 157) \times 10^{-6}} = \frac{1.46}{70} = 20.8K$$

$r_p = 20.8 K$	ohms
----------------	------

8. Data for calculation of μ

Note: These switch positions are for the revised experiment in the latest edition.

	SWITCH A DOWN SWITCH B UP V_{out} (plate volts)	SWITCH B DOWN Read V_G (input volts) Switch to negative meter if necessary
POINT 1	Vary input POT for: $V_{out1} = 5$ volts	$V_{G1} = +0.08$
POINT 2	Vary input POT for: $V_{out2} = 2$ volts	$V_{G2} = -0.36$ volts

TRIODE CHARACTERISTICS

9. Calculation of μ

$$\mu = \left(\frac{V_{out 1} - V_{out 2}}{V_{G 1} - V_{G 2}} \right) \times \left(\frac{R_L + r_p}{R_L} \right) = \left(\frac{5 - 2}{0.08 + 0.36} \right) \times \left(\frac{22K + 20.8}{22K} \right) = 13.2$$

$$\mu = 13.2$$

10. Calculation of Gain $R_L = 22K$

$$K = \mu \left(\frac{R_L}{R_L + r_p} \right) = 13.2 \left(\frac{22}{22 + 20.8} \right) = 6.8$$

$$K = 6.8$$

The gain achieved in Experiment No. 1 with a 100K Load Resistance was -8.5. Using the formula for gain and the r_p and μ found for the tube, the gain is:

$$K = \left(\frac{R_L}{R_L + r_p} \right) = \mu \left(\frac{100K}{100K + 20.8} \right) = 13.2 \left(\frac{100}{120.8} \right) = 10.9$$

$$K = 10.9 \quad \text{for 100K Load Resistor}$$

11. How does this calculated gain, K, compare to the measured amplifier gain from EXP. No. 1 which used a load resistance of 100K?

The measured gain for the 100K resistor is 8.5. The calculated gain for 100K load resistor is 10.9.

12. How would you select R_L for maximum voltage gain?

Maximum Voltage gain is achieved when the load resistor is as large as possible. As a general rule, we may select a load resistor equal to 10 times the tube r_p . This will result in a gain of μ , the tube amplification factor.

13. What R_L would you select for maximum power gain (recall the Maximum Power Transfer Experiment.)

The Maximum Power Transfer will occur when the load resistor is equal to the Tube Plate Resistance r_p .

TRIODE CHARACTERISTICS

14. What is the gain for an R_L of 200K?

$$K = \mu \left(\frac{R_L}{R_L + r_p} \right) = 13.2 \left(\frac{200K}{200K + 20.8} \right) = \left(\frac{13.2(200)}{220.8} \right) = 11.9$$

15. What is the maximum voltage gain you could obtain using any load with this TRIODE?

The maximum voltage gain achievable with this Triode is , the Amplification Factor.
 $\mu = 13.2$

16. Calculate the Transconductance, g_m . The "dimension" is the "inverse" of OHM and is called a MHO.

$$g_m = \frac{\mu}{r_p} = \frac{13.2}{20.8K} \text{ mho} = 0.63 \text{ millimho}$$

PLATE CHARACTERISTIC CURVE

The triode is used in a Common Cathode Configuration and the plate characteristic of Plate Voltage versus Plate Current for various values of Grid Voltage is plotted. This characteristic curve can be used with a Load Line to determine the operating point of the amplifier.

1. Table of Voltages

Switch B UP
Switch A UP

Set V_{cc} (Vary $+V_1$)	Switch B Down SET V_G AND READ V_P				Calculate I_p			
	$V_G = 0$ Switch A Down A	$V_G = -.25$ B	$V_G = -.5$ C	$V_G = -.75$ D	I_p A	I_p B	I_p C	I_p D
8	Switch A UP $V_p = 3.98$	5.56	6.73	7.52	0.182	0.114	0.058	0.033
6	$V_p = 2.96$	4.20	5.30	5.82	0.141	0.082	0.032	0.022
4	$V_p = 1.83$	3.00	3.69	3.97	0.099	0.045	0.014	0.008
2	$V_p = 0.75$	1.54	1.01	1.98	0.056	0.021	0.005	0
0	$V_p = -0.39$	-0.13	-0.01	0	-0.017	-0.006	0	0

3. Graph of results.

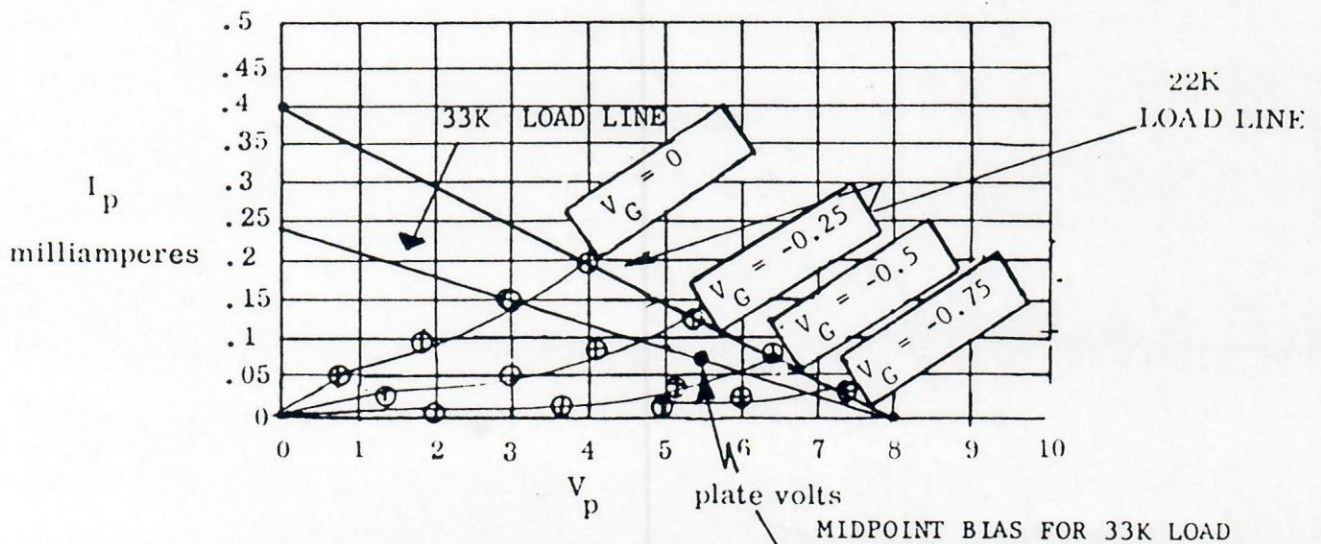


PLATE CHARACTERISTIC CURVE

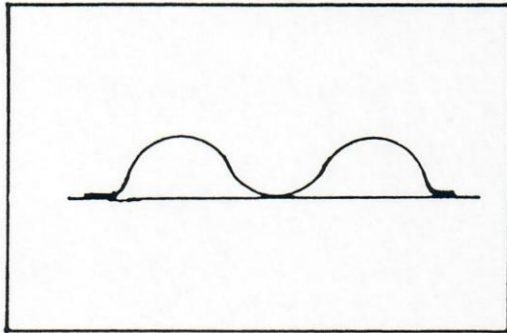
5. For the 33K load line the mid-point bias for the plate voltage is 5.5 volts.

The grid voltage that will result in 5.5 volts on the plate for a 33K resistor is estimated as -0.37 volts (note that the bias point falls between $V_G = -0.25$ and $V_G = -0.50$ volt curves).

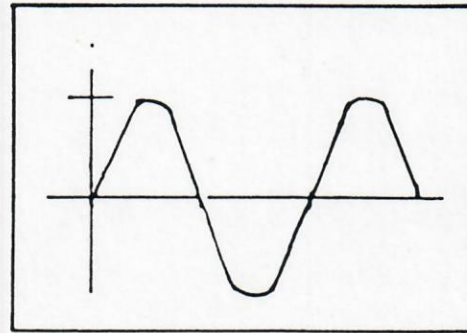
A.C. TRIODE GRID BIAS AMPLIFIER

The Common Cathode Triode Amplifier is connected with a Voltage Divider network to control the Grid Voltage. An A.C. signal is injected via a capacitor into the Grid circuit. The bias point is adjusted for undistorted output signal and the circuit gain is measured.

2. Waveforms



DISTORTED WAVEFORM



UN-DISTORTED WAVEFORM

3. Describe the effect of varying the BIAS (10K POT).

The adjustment of the Bias (10K POT) changes the D.C. level of the output voltage. When the triode is biased in the center of the available voltage swing the largest undistorted voltage output is obtainable. When the Bias voltage is adjusted so the D.C. plate voltage is near the maximum or minimum available power supply voltage the output signal decreases and becomes distorted.

4. Describe the effect of varying the INPUT (1K POT).

When the Input Amplitude (1K POT) is adjusted the output signal increases and decrease proportionally to the input signal. When the input amplitude is adjusted above the point where the Amplifier output voltage swing is exceeded the output signal becomes distorted.

5. Describe the effect of varying the LOAD (100K POT).

When the LOAD resistor (100K POT) is adjusted the output signal will increase and decrease. The gain of the circuit is proportional to the 100K POT setting. The larger the LOAD resistor the larger the circuit voltage gain. For small LOAD resistors the gain will be small.

A.C. TRIODE GRID BIAS AMPLIFIER

6. Data Table (Input and Output Voltages)

SWITCH A DOWN (NO-LOAD)	$V_{\text{input A.C.}}$	0.15 v p-p
	$V_{\text{output A.C.}}$	1.3 v p-p
UP (LOAD)	$V_{\text{out LOAD A.C.}}$	0.54 v p-p

$$\text{MEASURED GAIN} = \frac{V_{\text{out A.C.}}}{V_{\text{in A.C.}}} = \frac{1.3}{0.15} = 8.7$$

$$\text{THEORETICAL GAIN} = \mu \left(\frac{R_L}{R_L + r_p} \right) = 13.2 \left(\frac{50K}{50K + 20.8} \right) = 9.3$$

7. How do the measured and theoretical gain compare? Why is there a difference?

The gain for this amplifier and the theoretical gain differ slightly. The variation is due to the r_p and μ figures which were calculated for 22K LOAD resistance, may be slightly different.

CATHODE BIAS

A Cathode Resistor is placed in the Triode circuit to generate a Grid Bias Voltage. When Cathode Current flows in the tube the cathode resistor causes a voltage drop which makes the Triode Cathode assume a positive voltage. The Grid Voltage is then Negative with respect to the Cathode and the circuit is properly biased. Note that the Cathode Resistor must be by-passed with a capacitor to improve the circuit Gain (prevent Cathode Degeneration) just as the Emitter By-pass Capacitor was used in the Transistor circuit.

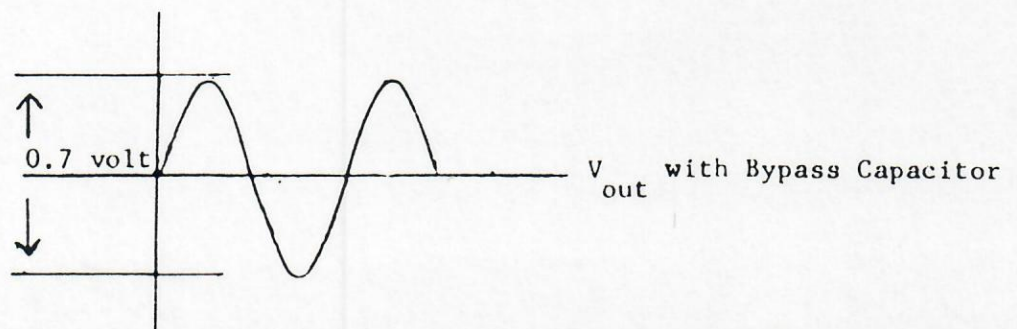
2. The Bias POT causes the D.C. operating point of the Triode to vary. When the input level is increased and decreased the output voltage also increases and decreases.
3. Compare the operation of this self-bias circuit with the operation of the grid bias circuit from the previous experiment.

The two circuits behave very similarly, the gains and waveforms are alike.

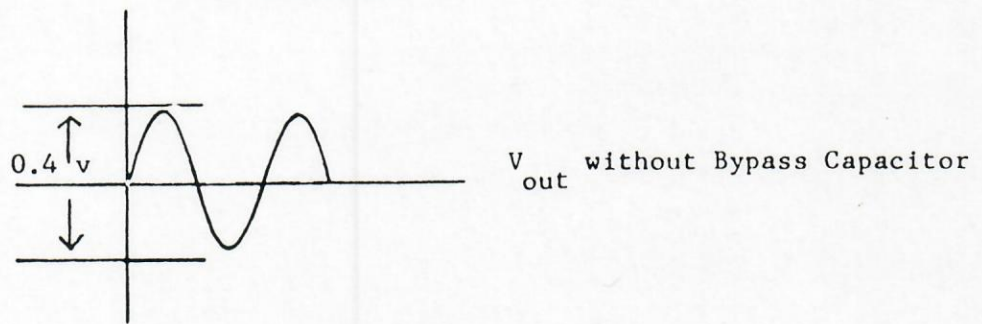
4. Data Table.

	MEASURE			CALCULATE
	V_{in} A.C. (pk to pk)	V_{out} A.C. (pk to pk)	V_K BIAS D.C.	$GAIN = \frac{V_{out} \text{ A.C.}}{V_{in} \text{ A.C.}}$
Test 1	0.1 v p-p	0.7 v p-p	0.4 v	$= \frac{0.8}{0.1} = 7$
Test 2 Remove bypass CAPACITOR	0.1 v p-p	0.4 v p-p	0.4 v	$= \frac{0.4}{0.1} = 4$

5. Output Waveform



CATHODE BIAS



6. Compare both Gains. Compare with the Gain in Experiment No. 4.

The Gain with the By-pass capacitor is 7, the Gain without the by-pass capacitor is 4. This reduction in Gain is a result of Cathode Degeneration, a part of the tube output voltage is developed across the Cathode resistor, causing a reduction in signal output at the plate. The gain of the circuit with the by-pass capacitor is comparable to the gain found in experiment No. 4.

7. Compare both Bias Voltages.

The Bias voltage is not affected by the removal of the capacitor because the Bias is D.C. and cannot flow in the capacitor.

CATHODE FOLLOWER AMPLIFIER

The Triode is used as a Cathode Follower. The primary features of the Cathode Follower are the same as those of the Transistor Emitter Follower. They are High Input Impedance, Low Output Impedance, Near Unity Gain and High Power Gain.

2. Data Table V_{in} and V_{out}

V_{in} A.C.	V_{out} A. C.
0.2 v p-p	0.15 v p-p
0.5 v p-p	0.4 v p-p
2 v p-p	1.6 v p-p
2.8 v p-p	2 v p-p
1 v p-p	0.75 v p-p

3. Gain Calculation

$$\text{Gain} = \frac{V_{out} \text{ A.C.}}{V_{in} \text{ A.C.}} = \frac{1.6}{2} = 0.8$$

$$\text{GAIN} = 0.8$$

4. Output Impedance

$$V_{out} \text{ A.C.} = 1.0 \text{ volts p-p}$$

5. Load Resistance for $\frac{1}{2}$ voltage out.

$$R_{output} = 0.5K$$

6. Input Impedance

$$R_{in} = 150K$$

Note: The load must be left at one setting when measuring the Input Impedance.

7. Power Gain

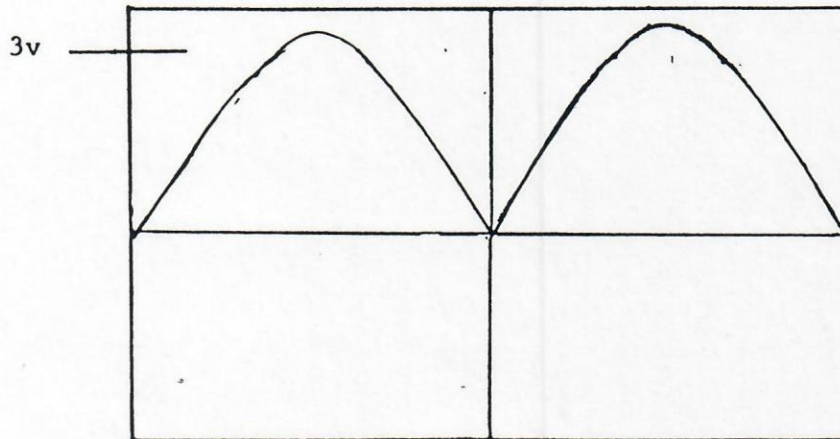
$$\text{POWER GAIN} = \frac{K^2}{4} \frac{R_{in}}{R_{out}} = \frac{(0.8)^2}{4} \frac{150K}{1.5K} = 16$$

$$\text{CATHODE FOLLOWER POWER GAIN} = 16$$

DIODE RECTIFIER

The Tube Diode is used in a Full Wave Rectifier circuit.

2. Cathode Voltage Waveform



3. How does this waveform compare with the semiconductor diode full wave rectifier?

The output waveform is identical to the full wave rectifier using semiconductor diode. The peak voltage is lower because the A.C. Input voltage is loaded by the tube heater.